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HIGH EFFICIENCY OCTAVE BANDWIDTH MILLIMETER WAVE POWER AMPLIFIER

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MM-Wave monolithic distributed amplifiers are designed to cover the 30-60 GHz frequency band. Both low-pass bandpass and negative resistance compensated designs are developed. The MMIC designs are based on psuedomorphic MODFET devices having 1/4 micron gates fabricated on 3-inch wafers using a hybrid e-beam/optical stepper lithography technique. In addition, to standard psuedomorphic MODFET structures with uniformly doped AlGaAs, psuedo-pulse-doped structures were also developed to address low drain breakdown voltage problems. 60 GHz monolithic gain cells with 10 mW output power were also developed.

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I. Introduction and Summary

This final report covers a two year period, or first phase of an originally planned five-year multi-phase program to develop highly efficient broadband mm-wave MMIC amplifiers in the 30-60 GHz range. The five year goal was to attain 1 Watt across this band. Much of the work accomplished during Phase I was motivated and guided by the longer term goals of the five year program. To effectively address the aggressive five-year goal, the technical work encompassed advanced techniques in materials growth, device and IC processing, and circuit development. For broadband performance at mm-wave frequencies, a distributed amplifier based on psuedomorphic MODFETs was chosen as the basic technical approach.

The objective and structure of Phase I was to develop a materials and device approach in parallel with analysis of advanced circuit techniques which would be combined in later phases of the program for the development of actual monolithic 30-60 GHz power amplifiers. For example, the objective of Phase II was to demonstrate a 40 mW 30-60 GHz amplifier, while Phase III aimed at a 200 mW realization prior to the development of the final IW amplifier. The specific goal for Phase I was to demonstrate a 60 GHz "gain cell" at 10 mW output power. These gain cells would form the basis for the development of the 40 mW amplifier during Phase II. Our program during Phase I included a preliminary design and layout for a 30-60 GHz distributed amplifier with an output power goal of 40 mW, i.e., the objective of Phase II. A significant portion of Phase I was devoted to the development of advanced circuit techniques for monolithic FET (and/or MODFET) distributed amplifiers which were aimed towards improving the efficiency, power and gain-bandwidth products of such amplifiers. Operation of distributed amplifiers under class B, negative resistance compensation of the gate line, as well as band-pass distributed amplifier topologies were investigated. This work was done at the University of Wisconsin and is discussed in Section II of this report.

Our materials approach was based on MBE growth on 3-inch wafers of strained layer (psuedomorphic) InGaAs channel MODFET material suitable for fabrication of large area circuits such as required for the typical distributed amplifiers envisioned for this program. Both "conventionally" doped and pulse-doped structures were successfully grown during this program. The pulse-doped MODFET structures are particularly suited for power FET applications where higher breakdown voltages are required. Although the initial monolithic circuits fabricated during Phase I (including the 60 GHz 10 mW gain cells) used a hybrid optical-contact/e-beam lithography approach, our second mask set which was prepared for early initiation of Phase II activities, was based on an advanced optical 10:1 projection e-beam hybrid lithography. This technique has the distinct advantage over contact mask techniques in that local precise (~ 0.2 microns) alignment of mask layers is accomplished on each of the 50 reticles defined on a 3-inch wafer. Alignment run-out

across the mask is, therefore, eliminated. For large area monolithic circuits this feature is critical for high yield across the wafer. With this approach, e-beam lithography is restricted to writing only the 0.25 micron gates of the FETs. At the conclusion of Phase I, we had completed the layout of our second mask set which included the design of a 30-60 GHz 40 mW distributed amplifier.

In addition to the circuit design, work was also directed towards the development of a broadband mm-wave test fixture that would be suitable for testing at least octave bandwidth mm-wave IC's. To this end several design possibilities were investigated and a preferred coaxial test fixture was chosen for use in Phase II. This fixture makes use of the latest available high frequency coaxial connectors recently introduced on the market. A design was completed for a 30-60 GHz test fixture using these latest coaxial connectors.

Specific accomplishments and highlights of the two-year effort in materials development, device and MMIC fabrication, and circuit analysis are summarized below.

o Materials Development

Four MBE growth runs were completed on 3-inch GaAs substrates. The epitaxial material was based on a strained layer (psuedomorphic) InGaAs channel MODFET device structure suitable for mm-wave frequency power generation at 60 GHz. Growth run No. 2 incorporated a conventional structure with uniform doping in the AlGaAs charge supplying layer. With this material, our first successful 60 GHz 10 mW monolithic amplifier was fabricated (see description below). However, the breakdown voltage of the MODFET devices was rather low (in the 3-4 V range) and limited the power capability of these first IC's. To remedy the situation a pulse-doped structure (100 A $Al_{0.2}Ga_{0.8}As$ with $N_D \sim 5 \times 10^{18}/cm^3$) was incorporated in growth runs No's. 3 and 4. Three, 3-inch wafers have been grown with a pulse-doped double heterostructure for improved current carrying capacity (two doping pulses are used on either side of the high mobility InGaAs channel layer). Typical sheet carrier density and mobility values for this material are $n_s = 4 \times 10^{12}/cm^2$ and $\mu = 4100$ cm^2/V-sec, respectively. These 3-inch wafers were to be used for the 30-60 GHz, distributed amplifier of Task II.

o Device and IC Fabrication

A mask set designed in 1987 and MBE material from growth run No. 2 was used to fabricate our first 60 GHz monolithic amplifiers (gain cells). Hybrid optical contact/e-beam lithography, nominally incorporating 0.25 micron e-beam defined gates, was employed for this mask set. A single-stage 60 GHz amplifier with small signal gain of 4 dB and a saturated output power of 12 mW was demonstrated from the devices of this processing run.

A drawback to the contact/e-beam process is that for larger, more complex circuitry, e.g., our 30-60 GHz distributed amplifier, the yield is very

low due to contact mask run-out and consequent misalignment as well as contact induced lithography defects. For this reason, we have translated our 30-60 GHz circuit designs over to a 3-inch format suitable for the stepper/e-beam process. This mask set was planned for fabrication of 60 GHz MMICs in Phase II.

o Advanced Circuit Analysis (University of Wisconsin)

During the Phase I of the project we analyzed and designed several advanced distributed amplifiers operating in the range 30-60 GHz and having the specified gain and output power. The designs incorporating common gate negative resistance attenuation compensating circuits in the distributed amplifiers to increase the gain-bandwidth product as well as output power succeeded beyond our original expectation and the work has been chosen for publication in the IEEE-MTT Special Issue on GaAs Structures scheduled for September 1989. The other novel designs accomplished during this period are: 1. cascode and compensated cascode distributed amplifiers, 2. band-pass distributed amplifiers, a novel concept that we developed after beginning work on this project. We conducted extensive experiments on single ended class-B amplifiers to ascertain the efficiencies obtainable from them. These experiments gave us insights into the device design (pinch-off characteristics and breakdown voltage requirements) for class-B amplifiers. We have shown that power-added efficiencies greater than 50 percent are obtainable by proper design of the device. We also developed non-linear models of MODFETs suitable for computer aided design of class-B amplifiers. Had this work continued as scheduled, considering the goals that were surpassed in Phase I, we are confident that the original goals set for the entire project would have been met and probably also surpassed.

o Test Fixture Development

To accommodate the anticipated testing of broadband mm-wave MMICs during later phases of the program, a design of a 30-60 GHz test fixture was completed. The fixture utilizes newly available 1.8 mm air dielectric coaxial connectors usable from DC to 65 GHz.

At the conclusion of Phase I, it was determined by the ONR Scientific Officer that funding for Phase II was not available. On-going work in process development, circuit analysis and test were brought to a conclusion, and the delivery of two 60 GHz gain cells in test fixtures was completed.

II. Circuit Analysis and Development (UW)

The long term goal envisaged is an octave bandwidth amplifier operating in the mm-wave spectrum (30-60 GHz) and having power-added efficiency greater than 50 percent. A distributed amplifier topology was chosen because of its wideband capability and class-B operation was selected in order to achieve the specified efficiency.

Task I of the project required the demonstration of a 30-60 GHz class-A amplifier module having a gain of 4 dB at 60 GHz and an output power of 10 mW. A four-section distributed amplifier using Honeywell CG-96 MODFETs was designed to meet this goal. Since the output power of this amplifier is limited and keeping in mind the power requirement (40 mW) for Phase II Option I, we investigated new design techniques such as negative resistance compensation on the gate-line (to overcome gate-line attenuation) and the cascode configuration (to overcome drain-line attenuation) [1]. These techniques showed promise of achieving higher output powers over 30-60 GHz range using GC-96 MODFETs.

We also investigated band-pass topology for distributed amplifiers for operation in the mm-wave range [2]. These amplifiers have the advantage of being able to operate beyond the cut-off frequencies of the conventional Low-Pass Distributed Amplifiers. The gate-line attenuation is, however, a gain-limiting factor at high mm-wave frequencies. The negative resistance compensation of gate-line attenuation has been found to be effective in obtaining flat gain response. We have designed a Band-Pass Distributed Amplifier in the 30-60 GHz range using GC-96 MODFETs and negative resistance compensation on the gate-line. The amplifier has a gain of 5 ± 1 dB over the band.

In order to understand the design of class-B amplifiers as well as ascertain the device requirements and design tradeoffs, we designed and tested single ended hybrid MIC class-B amplifiers. To achieve the high efficiency of class B amplifiers, one must return the even harmonic currents to the device at the FET drains. This ensures a half-sine wave current wave form at the drain while the drain voltages goes through a complete swing. We could accomplish this by means of a quarter-wave length (at the fundamental frequency) short-circuited stub at the drain [3]. Extensive load-pull measurements were performed on these circuits. It was found that due to "soft" pinch-off of the device true class-B operation was not obtainable. However, under class-AB operation, drain efficiencies of 69 percent at 3.8 dB gain and power-added efficiency of 55 percent at 4 dB gain compression were measured. These experiments were done at 9 GHz. The experiments revealed the importance of obtaining devices having good pinch-off characteristics for class-B operation. The efficiencies obtained are promising. Another important requirement of the device for class-B operation is the high break-down voltage between gate and drain. The voltage between gate and drain reaches an absolute maximum during the gate voltage swing beyond pinch-off.

The gain of a single ended class-B amplifier is 6 dB lower than a class-A amplifier. This is due to half-sine wave drain current in class-B amplifiers. The 6 dB loss in gain can be recovered by using the classical push-pull configuration. The push-pull amplifiers need to be fed in balanced fashion and the output signals combined to provide an unbalanced output. Therefore, one needs baluns to accomplish this. We have made studies on baluns that could operate over octave bandwidths in the mm-wave region.

We have investigated the modelling of MODFETs under class-B operating conditions. We have successfully generated a non-linear circuit model suitable for computer simulations using the measured small signal s-parameters at several bias conditions. The model was verified experimentally [4].

During Phase I of the project several test circuits were designed for fabrication on Mask Set #1. A brief explanation of these circuits and an elaboration on the accomplishments summarized above will be presented in the following paragraphs. For details of some of the tasks accomplished the interested reader is referred to the copies of the publications in the Appendix.

A. Circuits Designed for Mask Set #1

1. Class-A 30-60 GHz Distributed Amplifier (DA)

During the period of Task I an octave bandwidth amplifier operating under class-A conditions up to 60 GHz and providing a gain of 4 dB and an output power of 10 mW was required to be designed and tested. The natural choice for broadband power amplification is a Distributed Amplifier (DA). A DA meeting the foregoing specifications was designed using the 0.25 x 100 micron MODFETs (GC-96) developed by Honeywell.

A DA topology utilizing monolithically integrated discrete FETs was chosen for the design. Traveling Wave FET (TWF), an alternative to the use of discrete transistors in DA design, has been suggested in the literature. In a TWF the signal is continuously amplified as it travels along the bulk material. The disadvantages of this configuration are two fold: i) the gate-source volume causes attenuation of the input driving signal, resulting in insufficient excitation of down stream device volume. Not only does unexcited device volume no longer contribute to the output wave, but inactive drain-source volume acts as a series attenuator, hence total useful device length is limited. ii) Due to the small physical size of a TWF one encounters low RF impedance levels at input and output ports. The afore mentioned limitations of a TWF are overcome in a DA designed using discrete FETs. In a properly designed discrete transistor DA, compensation in part for the input line attenuation is provided by the voltage increase with frequency seen at the π-section terminals of a lumped element constant-k transmission line. Further, DAs have been designed and demonstrated to operate at 50

ohm input and output impedance levels. Therefore, we selected a DA configuration using discrete transistors for Task I of the project.

The CALMA generated layout of the DA designed using four 0.25 x 100 micron MODFETs is shown in Fig. 1. 90 ohm microstrips were used on the gate-line and 80 ohm microstrips on the drain-line. The gate and drain-lines were designed to be 50 Ω lines. Gate-series capacitors (0.15 pF) and gate DC bias resistors (~ 500 Ω) were used as shown. The gate-series capacitors and gate dc bias resistors were realized as MIM capacitors and floating gate transistors respectively. The gate and drain dc bias voltages were applied through the terminated ports on gate and drain lines. The on-chip bias networks were designed as 2-section Chebyshev low-pass filters. The computer simulations showed a gain of 4 dB in the range 30-60 GHz and input and output return losses better than 10 dB in the band.

We were able to obtain the specified gain and bandwidth by the use of gate-series capacitors. Gate-series capacitors enable one to reduce the gate-line attenuation and hence allow more transistors in the amplifier. They also enable one to increase the input power capability by allowing larger input voltage swing. They, however, reduce the gain per device and hence the overall gain of DA (because of the voltage division between the external series capacitors and the internal capacitance of the device) which is however, compensated for by the additional number of devices which can be connected without sacrificing the original bandwidth.

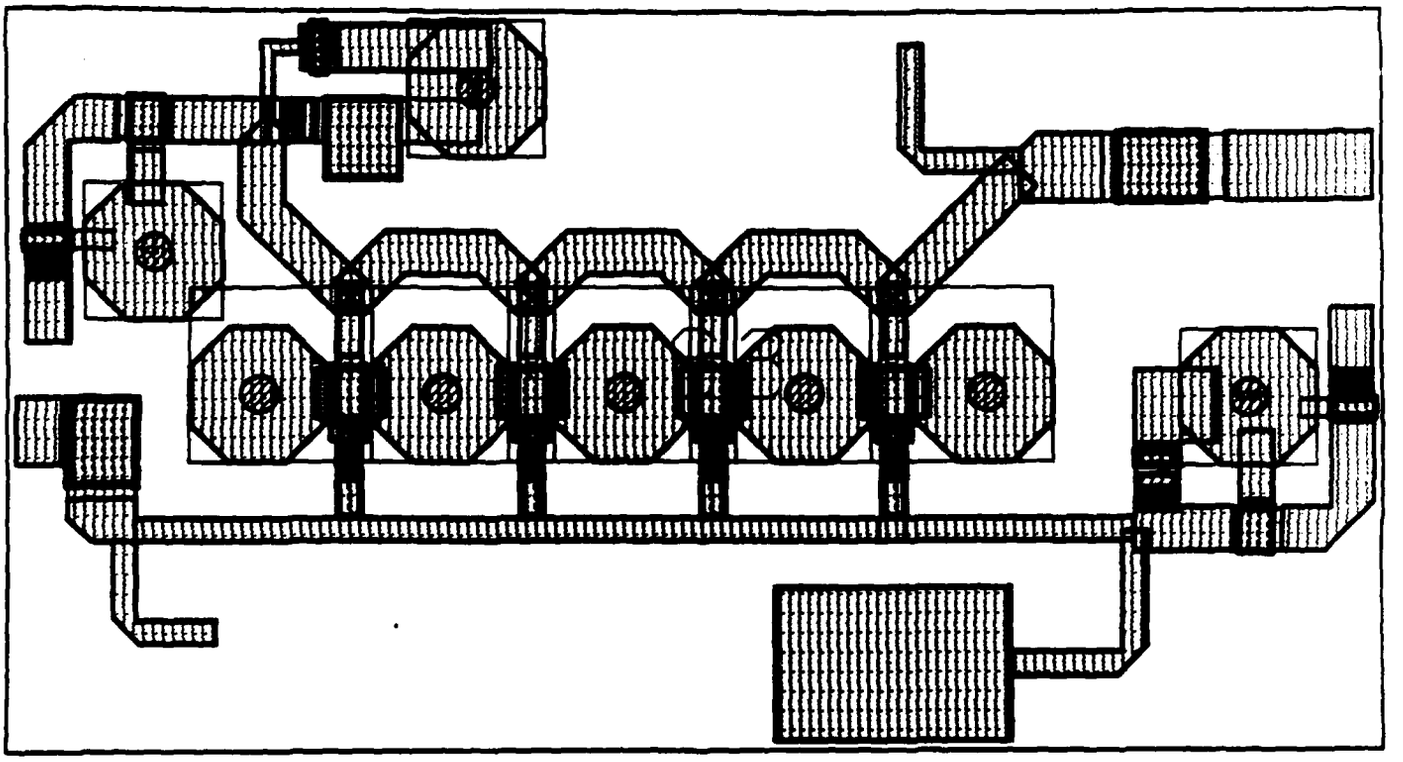


Fig. 1. Layout of class-A 30-60 GHz DA using CG-96 MODFETs.

2. Gate Parallel R-C Cell

This is a test cell designed for the purpose of characterizing the gate parallel R-C circuits present in the class-A 30-60 GHz DA described earlier. The test cell is designed to be tested in the range 2-18 GHz. The data obtained from the experiment will enable one to model the cell accurately.

3. Image Impedance Transformer

This is a circuit used in the class-A, 30-60 GHz DA to provide the impage impedance termination at all four ports. The measurement of reflection and transmission characteristics of this test cell over the range 2-18 GHz will provide useful design information.

4. DC-Bias Circuit

This test circuit is a 2-section (4 element) Chebyshev Low-Pass filter used in 30-60 GHz class-A DA. This circuit isolates the DC source from RF signals. It is a part of drain and gate terminating network. Measurement of reflection and transmission characteristics of this circuit is essential to develop useful design criteria for such networks. Since there was not enough room to accommodate this circuit on the wafer (Mask Set #1) it was decided to build this circuit in hybrid MIC form on Alumina substrate. The circuit has been designed to give a cut-off frequency of about 4 GHz.

5. Single-Section Class-B DA

The CALMA layout of the class-B test cell is shown in Fig. 2. This circuit is a section of the DA having a quarter-wave length (at the fundamental frequency = 13.5 GHz) stub at the drain of the 0.25 x 100 micron MODFET (GC-96). This test cell was designed keeping in mind the long term objective of the project - the design and performance evaluation of class-B DA. The following measurements of the circuit are envisaged: a) drain efficiency, b) S_{21}, S_{11} and S_{22} vs. frequency, c) harmonic content in the output.

6. Common Gate Negative Resistance Test Cell

The layout of this cell is shown in Fig. 3. This test cell is useful for the investigation of the negative resistance presented by a common-gate MODFET when terminated by a high RF impedance at its source. The high impedance is obtained by means of a quarter-wave length (at 10 GHz) stub with a large capacitance (radial stub) to ground. This circuit is needed in a DA to counter the detrimental effect of the device positive resistance on the gate-line. The measurement of input reflection coefficient (S_{11}) as a function of frequency will enable us to model this circuit accurately.

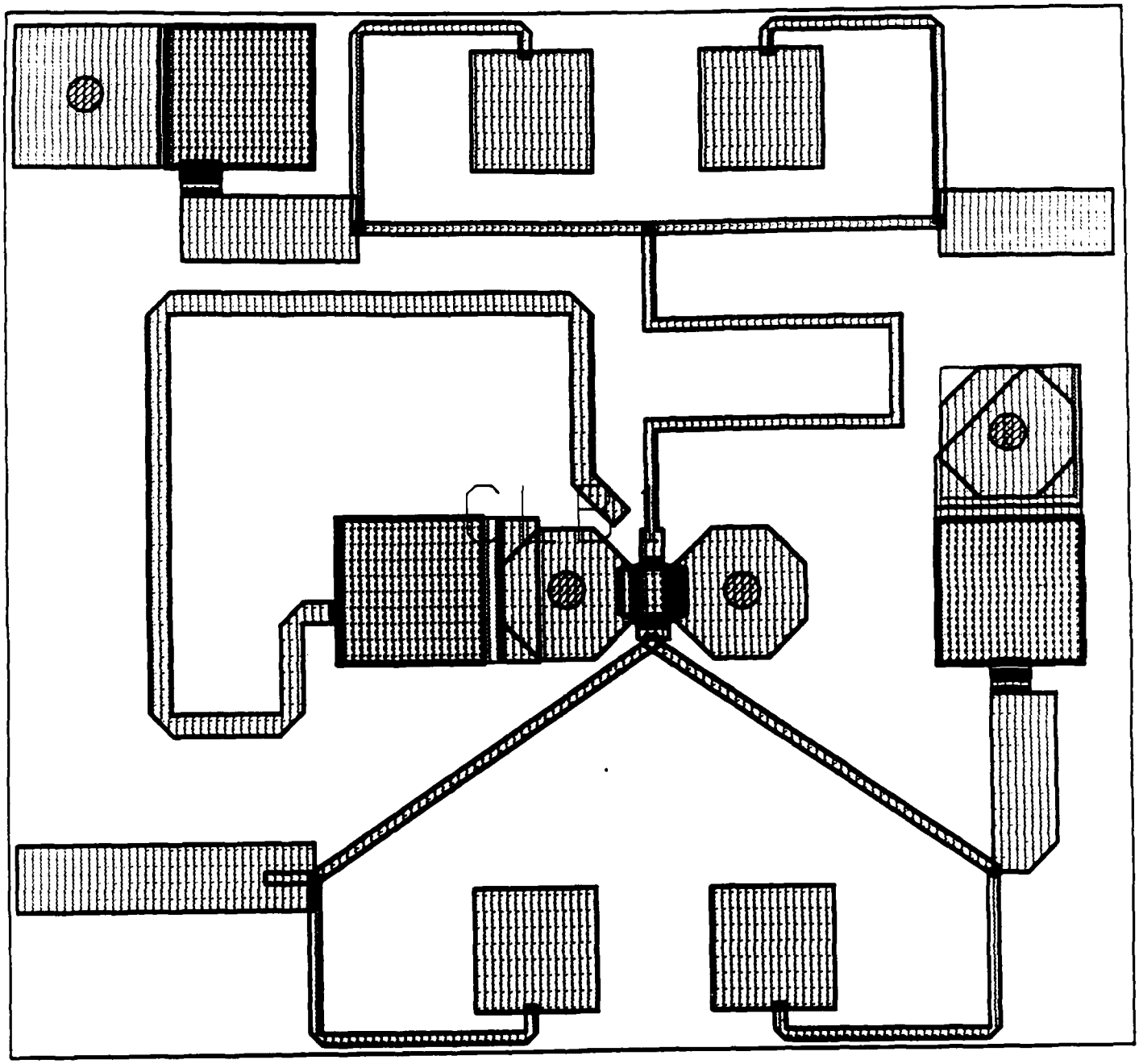


Fig. 2. Layout of single-section class-B DA.

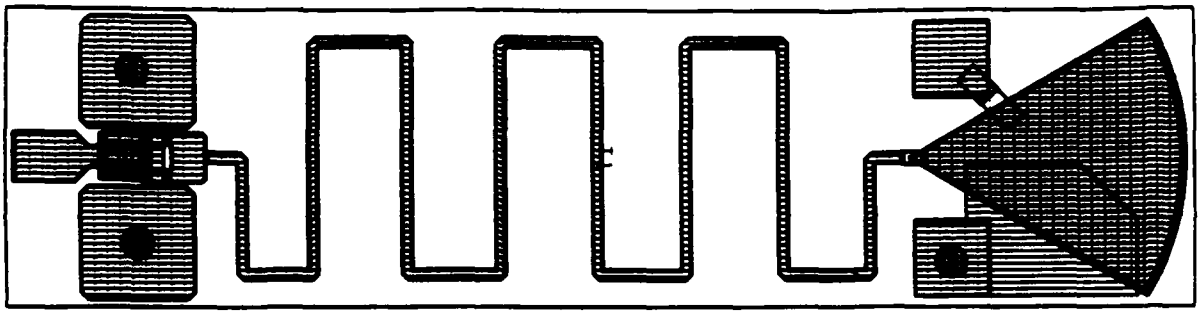


Fig. 3. Layout of common gate negative resistance test cell.

7. Cascode Test Cell

The layout of the cascode test cell is shown in Fig. 4. The cascode test cell resembles a dual gate transistor except for the transmission line present between the drain of the common source transistor and the source of the common gate transistor as shown in the figure. The cascode cell can be used as an amplifying device in a DA. The major advantage of the cascode configuration in a DA is its high impedance between drain and source which results in lower attenuation on the drain line. The drain-to-source impedance and transmission characteristics of the cascode cell depend upon the length of the transmission line between the transistors. The purpose of designing this test cell is to study its characteristics as a function of the transmission line length.

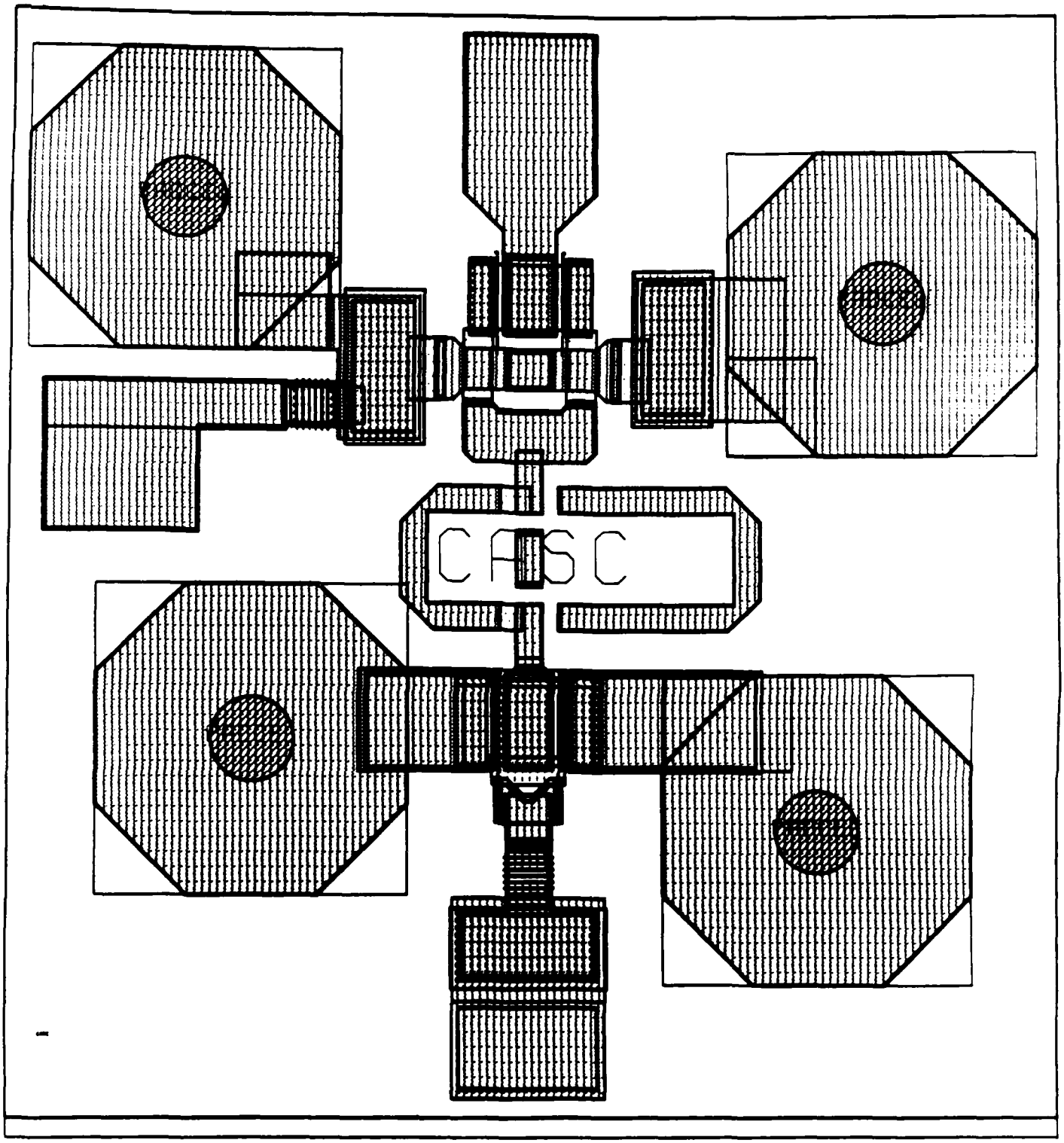


Fig. 4. Layout of cascode test cell.

B. Advanced MM-Wave Amplifier Designs

1. Attenuation Compensated Distributed Amplifier Designs

We have developed new design techniques to increase the gain-bandwidth and the gain-maximum frequency products of mm-wave Distributed Amplifiers [1]. It has been found that a high gain common gate FET can present at its drain a broad band impedance characterized by a frequency dependent negative resistance and a capacitance. This was examined both theoretically and experimentally. Loading the input and/or output lines of a distributed amplifier with this circuit reduces the signal losses, leading to an increase in the allowed number of active devices with a consequent increase in the gain-bandwidth and gain-maximum frequency products. The cascode circuit, a related loss reduction network, was also evaluated because of its use in Distributed Amplifiers. Several designs employing the common gate FET loss compensating circuit and/or cascode amplifying circuits were designed and studied. The use of negative resistance loss compensation on either of the two DA lines was found to substantially increase the single stage gain-bandwidth product performance as compared to the maximum product possible with conventional DA designs. The impact of this performance enhancement is two-fold: Improvements in the single stage gain often promise increased maximum output power, while increases in bandwidth are desirable for modular system design.

2. Band-pass Distributed Amplifier Design

We have designed and analyzed [2] the Band-Pass Distributed Amplifier topology for applications in 30-60 GHz range. Band-Pass Distributed Amplifiers can be designed to operate beyond the cut-off frequencies of the conventional Low-Pass Distributed Amplifiers. The topology is well suited for GaAs monolithic circuits. The schematic of the amplifier is shown in Fig. 5. The amplifier has a gain of 5 $\pm$ 1 dB over 30-60 GHz (Fig. 6) and a nearly linear phase response (Fig. 7) in the band. At high mm-wave frequencies severe gain roll-off occurs due to high gate-line attenuation. This detrimental effect, however, can be overcome by the use of negative resistance attenuation compensation techniques described earlier.

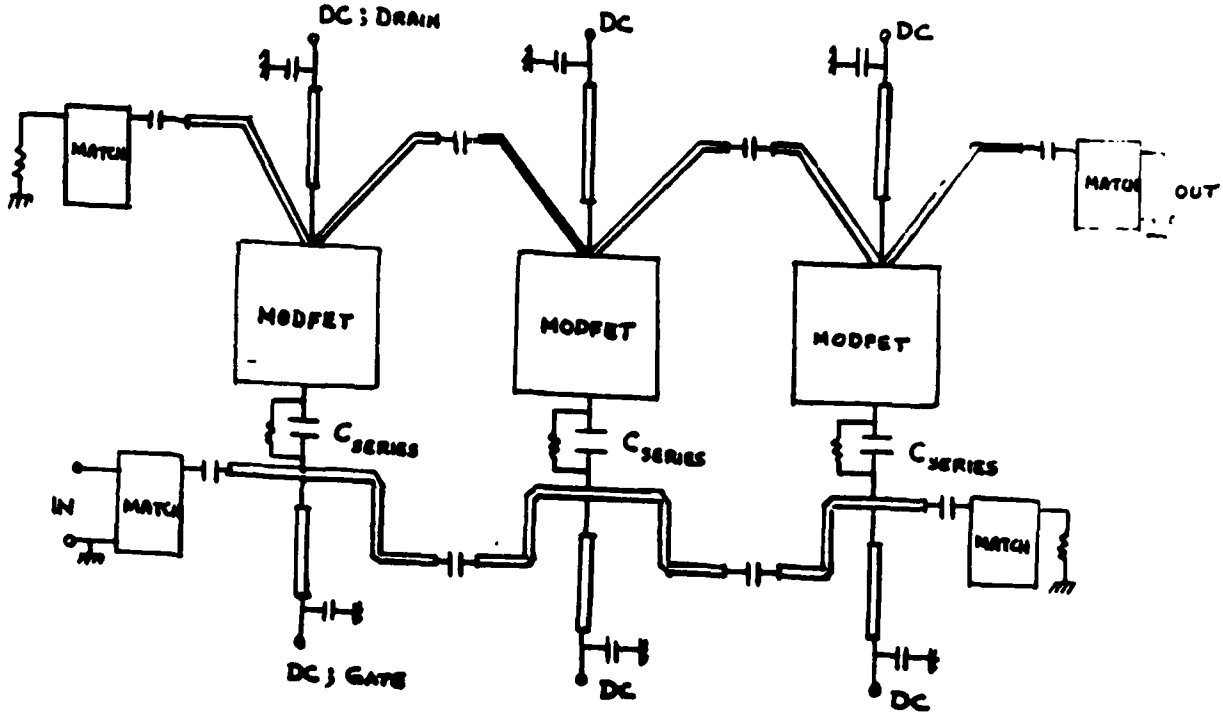


Fig. 5. 30-60 GHz band pass dis. amplifier

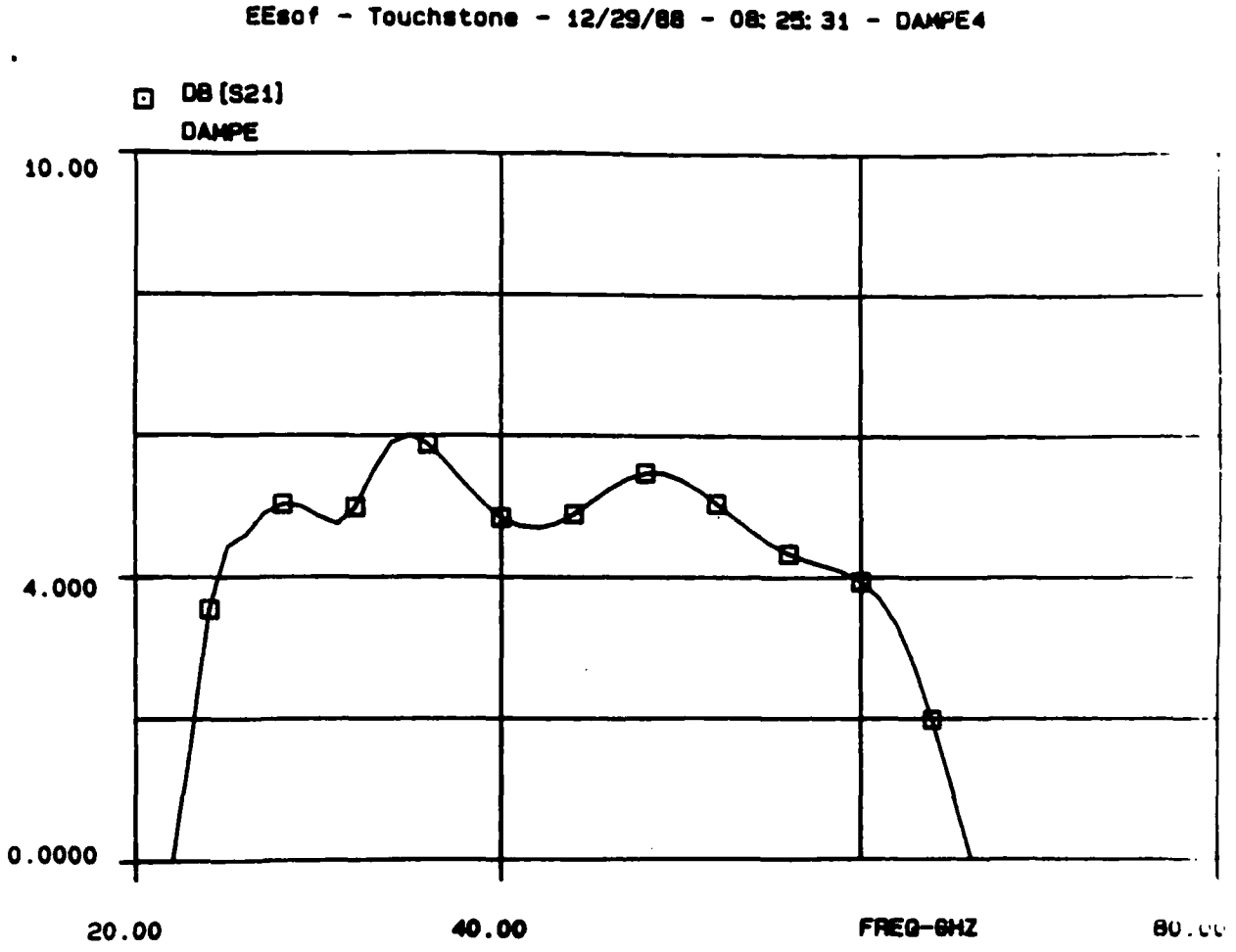


Fig. 6. Gain response of 30-60 GHz band pass DA

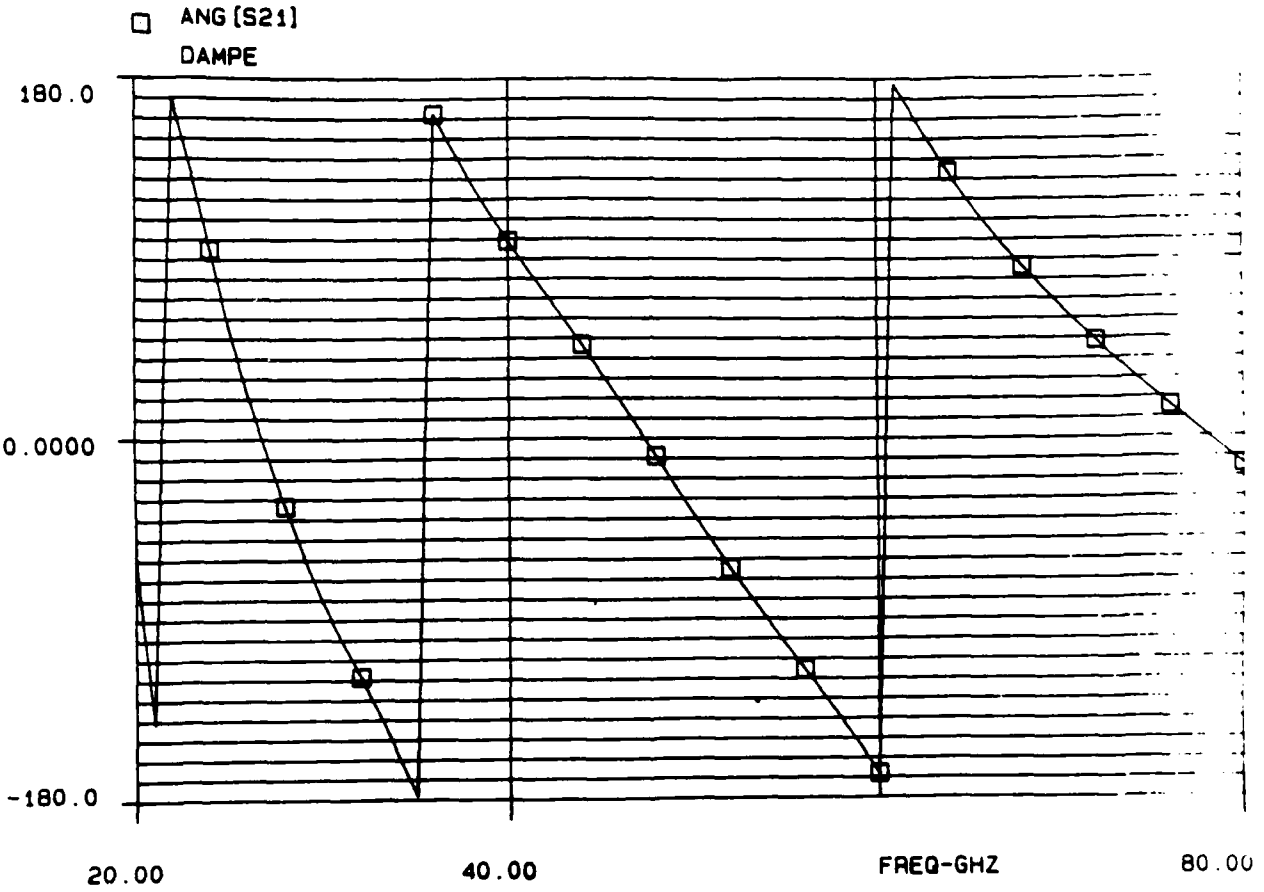


Fig. 7. Phase response of 30-60 GHz band pass DA.

C. Class B Hybrid Amplifier Testing

Commercially available MODFETs were incorporated in 9 GHz hybrid MIC amplifiers and measurement were made under high efficiency operating conditions approaching Class B operation. Because of the "soft" pinch-off characteristics of these devices, true Class B operation was unobtainable. Nevertheless, high drain efficiencies were obtained by biasing the device at reduced idling drain currents (14 mA vs. 32 mA I_{DSS} with no rf signal input) and operating it under large signal drive. Both input and output tuners were used to provide optimum impedance match. This Class "AB" operation resulted in power added efficiencies over 50% and a drain efficiency as high as 60%. The following Table I shows the measured results.

Table 1

High Efficiency Operation of MODFET
(V_{DS} = 2.77V, V_{GS} = 0.25V, f = 9 GHz)

Pin (dBm)	Pout (dBm)	G Linear (dB)	I_D (mA)	Power-Added Eff. (%)	Drain Eff. (%)
13.1	16.9	3.8	25.5	41	69
10.8	16.8	6.0	25.2	50	68
7.9	16.4	8.5	24.8	55	64
5.7	15.8	10.1	24.2	51	56
4.8	15.5	10.7	23.9	49	53
3.5	14.8	11.3	22.9	44	48
-1.5	10.8	12.3	17.0	24	25

From Table 1, it is seen that a maximum power-added efficiency of 55% is obtained at 4 dB gain compression, while the maximum drain efficiency is obtained at only 3.8 dB gain. In general, high efficiency is obtained in the non-linear region of the gain characteristic. Other measurements of Class AB operation under slightly different bias and frequency operating conditions have shown similar non-linearity in the gain characteristics, including some gain expansion prior to gain compression at high drive levels. These measurements indicate the importance of having good pinch-off characteristics for true Class B operation. We believe that "flat" g_m versus gate voltage with no premature breakdown in the device characteristics near pinch-off must be achieved before one can exploit the benefits of true Class B operation. In summary numerous positive results well beyond those originally proposed for Phase I were obtained. These results indicate a high probability of success of the original proposal and the work should continue.

III. Materials and Process Development

o Materials and Fabrication Process Approach

The materials approach selected for the originally planned five-year multi-phase program centered on molecular-beam epitaxial (MBE) grown psuedomorphic InGaAs channel MODFET material. At the outset of the first phase psuedomorphic InGaAs channel material growth had only been reported on small GaAs substrates; however, the direction was clear for advances in material growth and we selected as our approach the MBE growth of InGaAs MODFET material on full 3" substrates. Uniform, large substrate growth is a necessity for development and demonstration of actual 30-60 GHz distributed amplifiers, as required for later phases of the power amplifier program, because these circuits are large and dense.

The first phase (MBE materials/device/process) goals were to develop capability for the (planned) five year distributed power amplifier and demonstrate this capability with delivery of 60 GHz 10 mW "gain cells". These "gain cells" would form the basis for development of second phase 40 mW distributed power amplifier. The fabrication approach we chose for the first phase was a hybrid e-beam/contact lithography sequence in which the full 3" MBE wafers were quartered. Fabrication of the gain cell, test structures, discrete FETs and circuits described in Section II were executed on 2 or 3 wafer quarters. At least one wafer quarter from each wafer grown was evaluated for materials properties. This approach allowed feedback on materials growth from each wafer grown and no separate growth runs to optimize the 3" MBE material were initiated. As processing progressed, it became clear that the 1/4 wafer hybrid e-beam/contact lithography sequence was not adequate for circuit fabrication due to alignment problems, mask run-out, resist edge-beading and breakage. The design layouts were then reassembled in 8.4 mm square reticles for planned purchase of a projection lithography mask to allow fabrication with a direct wafer-stepper/e-beam (gate) fabrication process. A 40 mW 30-60 GHz distributed amplifier was included. At the conclusion of phase I, this mask set was being prepared for purchase for the second phase of the program.

o Materials Development

The first MBE material growth run began in October 1987. Growth on slices 826-830 was completed and evaluated in the next four weeks. The device layer structure grown is illustrated in Fig. 8.

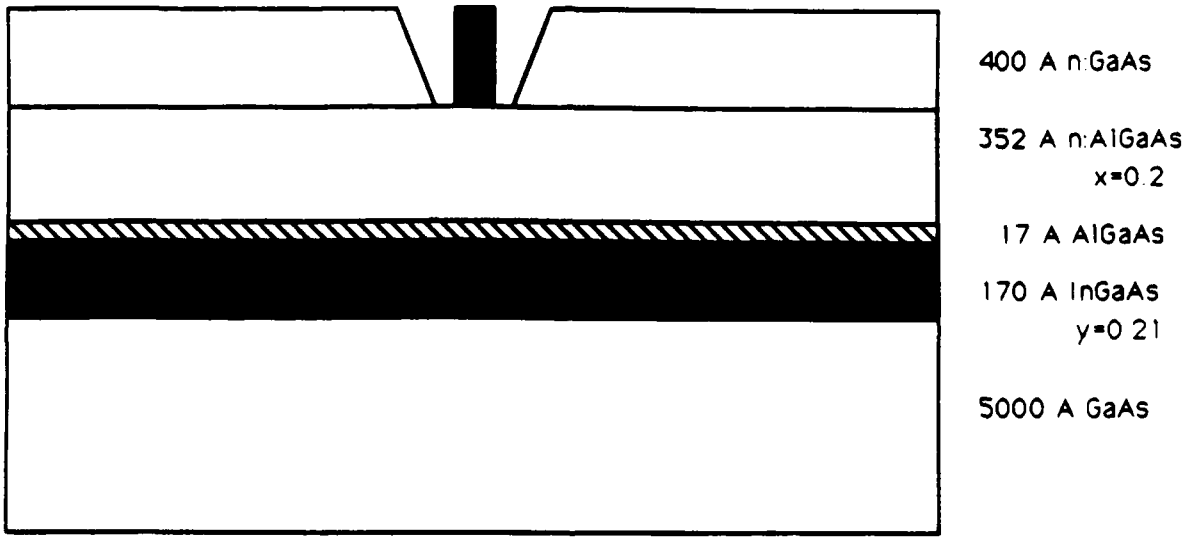


Fig. 8. Stanard psuedormorphic InGaAs channel MODFET layer structure.

Hall measurements on these samples proved disappointing. Room temperature sheet carrier densities and mobilities were characteristic of the n:GaAs cap only suggesting very little active dopant in the n:AlGaAs charge donation layer. The problem was isolated to the wafer temperature during AlGaAs growth being too low, causing inadequate dopant activation. The difficulty arose because the optimum growth temperature for InGaAs and n:AlGaAs are very different with higher quality InGaAs preferring a lower growth temperature and higher quality doped AlGaAs preferring a higher growth temperature. At the time of the wafer growth MBE wafer mounting procedures were changing from "indium" mounting to "indium free" mounting and uncertainty in substrate temperature was at fault. No fabrication on the first growth run was attempted. Under Honeywell IR&D funds, a set of calibration samples was established in January 1988 in preparation for the secod growth run.

The second MBE material growth run began in February 1988 and yielded successful material device and circuit results. In addition to three wafers (numbered 877-879) grown with the conventional GaAs buffer layer, two additional wafers (numbers 880, 881) added an additional feature to attempt to improve substrate conduction effects that had been identified under IR&D growth runs. The problem that had showed up were "kinks" in drain IV characteristics, characteristic of buffer conduction at drain voltages above 5 V. Since the power MODFETs were designed to operate out to 9V at the drain, a superlattaice GaAs/AlGaAs buffer layer was added to wafers 880 and 881 to attempt to reduce this effect.

The layer structure with SL buffer is illustrated in Fig. 9. The AlAs mole fraction was dropped to 0.17 in the n:AlGaAs charge-donation layer:

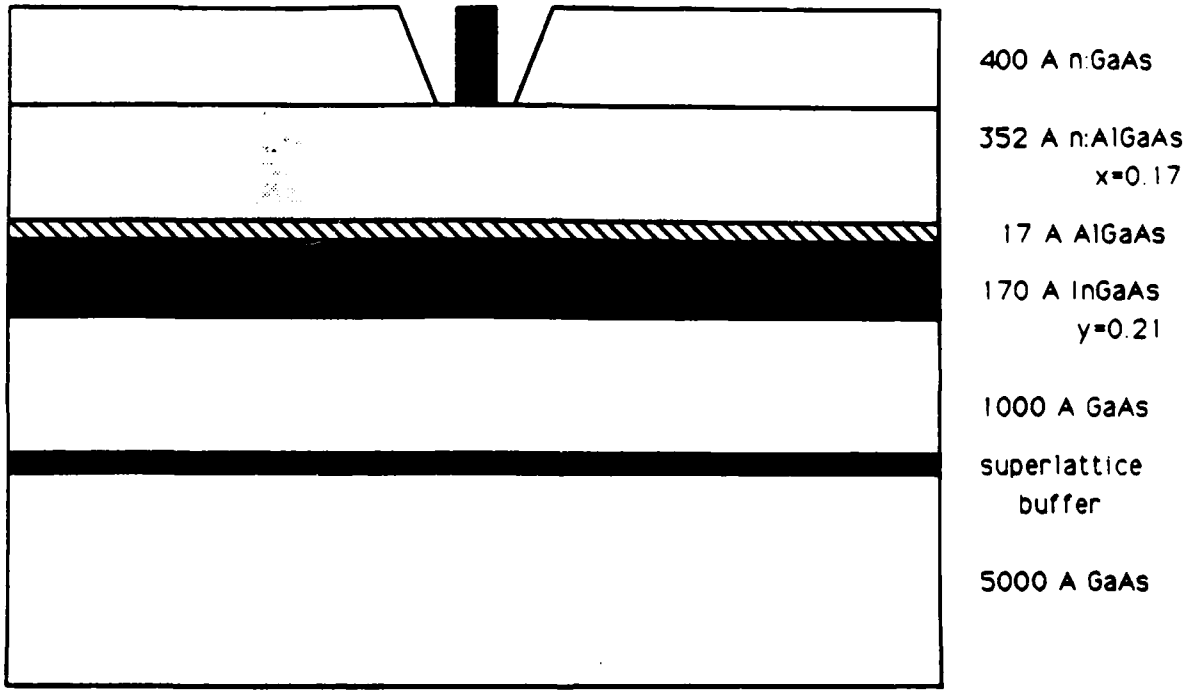


Fig. 9. MODFET layer with GaAs/AlGaAs (24A/72A) superlattice to reduce substrate conduction.

and the InAs mole fraction in the channel region was reduced to 0.19 in addition to having the thickness reduced from 170 to 155 A in the second growth run. Calculations show the current conduction will be weakly affected by the reduction of the InGaAs channel thickness. However, the combination of lower InAs mole fraction and thinner layer reduces the possibility of dislocations occuring in the channel, since the strained InGaAs layer is well below the critical thickness - the thickness above which dislocation relax the InGaAs strain. Materials properties are listed in Table II.

TABLE II

	Room Temp.			77K		
Wafer	Carrier Sheet cm^{-2}	μ cm^2/Vs	Rsheet	Carrier sheet cm^{-2}	μ cm^2/Vs	Rsheet
877	2060	$9.45\ 10^{12}$	321	6720	$4.94\ 10^{12}$	188
878	2073	$10.5\ 10^{12}$	286	8223	$4.61\ 10^{12}$	164
879	1834	$10.4\ 10^{12}$	327	7112	$4.76\ 10^{12}$	184
880	1204	$17.1\ 10^{12}$	303	3055	$9.43\ 10^{12}$	217
881	1505	$14.6\ 10^{12}$	283	4220	$8.27\ 10^{12}$	179

Fabrication began on these wafers and 60GHz monolithic amplifiers were successfully fabricated. FET dc and rf characteristics and 60 GHz gain cell results are reported below. Low breakdown voltage limited the power capability; and FET gate lengths slightly larger than the target 0.25 μm were produced, causing some high frequency gain degradation.

The third MBE material growth run begain in May 1988. In addition to 2 "standard" psuedomorphic MODFET structures with uniformly doped AlGaAs, 3 psuedo-pulse-doped MODFET layers (Fig. 10) were also grown to address a low drain breakdown voltage problem. By confining the doping in the AlGaAs to a thin layer, after recessing the gate metal contacts undoped AlGaAs rather than heavily doped AlGaAs.

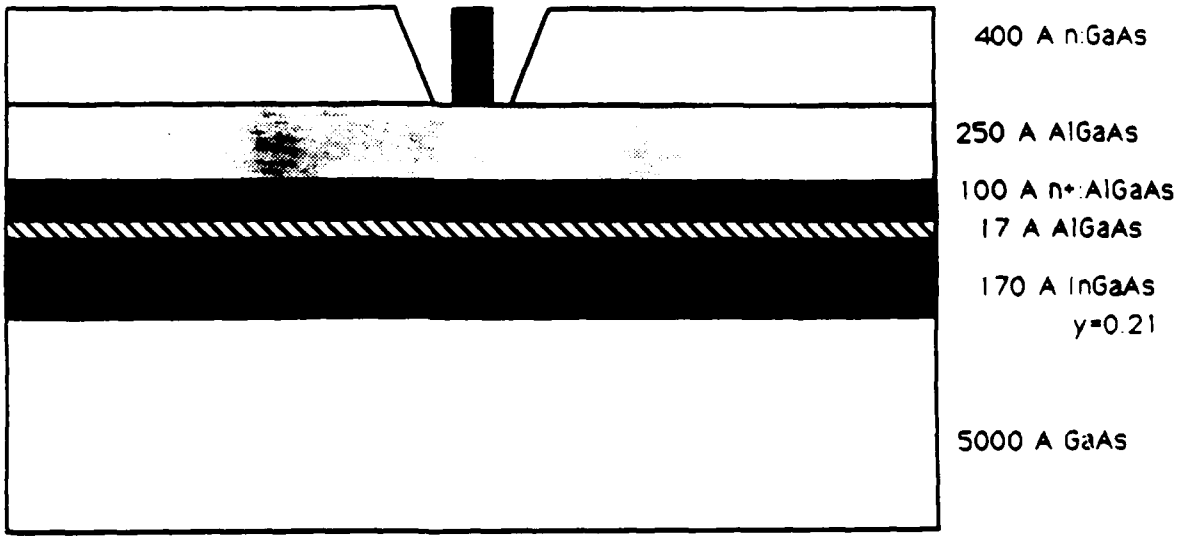


Fig. 10. Psuedo-pulse doped InGaAs channel MODFET, to improve breakdown voltage, the gate contacts undoped AlGaAs.

The undoped AlGaAs provides a lower leakage gate and supports higher drain breakdown voltages.

Fabrication began on these wafers in July 1988 and 60 GHz gain cells with performance slightly superior to those fabricated from MBE growth run #2 resulted. Unexpected difficulties with high ohmic contact resistance and only marginal breakdown voltage improvement were seen.

Material data from this growth run is tabulated in Table III. Note that the cap doping is high (~ 6 and 10^{18} cm^{-3}) which causes the measured layer mobilities to appear low and sheet carrier densities to appear high.

TABLE III

		Room Temp.		77K	
Wafer	Structure	ns cm^{-2}	μ cm^2/Vs	ns cm^{-2}	μ cm^2/Vs
394	Standard	2.44 10^{13}	1236	1.62 10^{13}	2293
395	Standard	3.85 10^{13}	844	3.40 10^{13}	1049
397	Psuedo-pulse	2.36 10^{13}	911	1.96 10^{13}	1231
398	Psuedo-pulse	3.23 10^{13}	1014	3.04 10^{13}	1154
399	Psuedo-pulse	2.35 10^{13}	931	2.25 10^{13}	1024

The fourth MBE growth run was preceded by a number of development growths (layers not suitable for circuit fabrication) to establish growth techniques to eliminate trapping effects in AlGaAs which were causing calibration difficulties. These trapping effects were apparent when Hall measurements of MBE layer doping were compared to doping densities determined by capacitance-voltage. The study examined variation in substrate (growth) temperature, Si flux, and III-V ratio during growth (As pressure). A more limited study of changes in x and y values for the $Al_xGa_{1-x}As$ and $In_yGa_{1-y}As$ growth were examined. Two conclusions were reached: First, our AlGaAs doping calibration were inconsistent and as a result we were doping, the AlGaAs higher than we thought. This almost certainly resulted in degradation of FET power output capability. Secondly, our materials quality and mobility measured without the heavily doped cap shunt, were comparable to the best reported, when growths used conservative InAs mole fractions in the channel.

The fourth MBE growth run was also split, with the first half being grown in the Perkin Elmer 430 MBE reactor, the usual reactor used for the ONR power amplifier growths, and the second half in the Perkin-Elmer 425. Under corporate IR&D programs, some evidence had been accumulating that suggested superior psuedomorphic InGaAs channel MODFET layers were grown in the 425. The first half of the fourth growth run was completed in

October 1988 and the second half in November 1988. Calibration growth run materials data (no n + GaAs cap) are reported in Table IV from the 430 half. All structures are of the psuedo-pulse doped type.

TABLE IV

	Room Temp		77K		
Growth	ns cm^{-2}	μ cm^2/Vs	ns cm^{-2}	μ cm^2/Vs	Comment
533	1.9 10^{12}	5570	2.1 10^{12}	24570	
534	2.2 10^{12}	4970	2.4 10^{12}	19330	
535	1.9 10^{12}	950	2.9 10^{12}	1670	x, y value too high
536	1.8 10^{12}	6075	1.9 10^{12}	24170	
537o	1.2 10^{12}	910	2.3 10^{12}	860	x, y value too high

Materials properties of the calibration wafers grown in the 425 (growth 48) are listed below in Table V. In addition to psuedo-pulse doped wafers double heterojunction pulse doped MODFET calibrations were also grown. We believe these structures are the most promising candidates for future full 3" mm-wave circuit power applications;

TABLE V

		Room Temp		77K	
Growth	Structure	ns cm^{-2}	μ cm^2/Vs	ns cm^{-2}	μ cm^2/Vs
1126	pulse-doped	1.8 10^{12}	5178	2.2 10^{12}	17680
1127	double HJ	2.9 10^{12}	3989	3.1	12140
1128	pulse-doped	2.1 10^{12}	4833	2.4	14050
1129	double HJ	4.0 10^{12}	4153	3.7	10180
1130	pulse-doped	0.83 10^{12}	5000	1.6	22070
1131	pulse doped	1.4 10^{12}	5625	1.8	21200
1138	pulse doped	1.0 10^{12}	5567	1.3	25200
1139	pulse doped	1.9 10^{12}	5730	1.9	20240

The materials properties are all good and in some cases excellent. Low field mobilities exceeding 4500 at room temperature with sheet carrier densities above 2 10^{12} are among the best reported. The addition of an added doping pulse beneath the strained InGaAs channel gives roughly a 70% increase in sheet carrier density to the channel with little low field mobility pending. The InGaAs channels were kept at 100 A for all the calibration growths in Table V. A cross section of the double-heterostructure InGaAs channel MODFET is illustrated in Fig. 11.

By the time fabrication was to begin on material from MBE growth run 4, we had already met the 60 GHz gain all requirements of phase 1 of the program and problems with the hybrid e-beam/contact lithography process had been identified. These problems affected FET yield and monolithic 60 GHz yield somewhat but there were still plenty of working circuits. However, the yield of the large 30-60 GHz amplifier circuit,added to the phase 1 mask set in preparation for phase 2 work was so low that fabrication through backside processig was judged to be a waste of resources. Instead, plans were made to switch to full 3" wafer fabrication, mask layout including the designs for phase 2 delivery were prepared and some wafers from growth run 4A were begun processing with an existing FET-only mask set to isolate fabrication problems with full 3" wafer psuedomorphic MODFET. This work was done in preparation for phase 2. FET results, reported in more detail below, were good but suffers from low channel current. We believe that in reducing the AlGaAs doping we undershot the target doping with this growth run and the problem has a clear solution.

At the end of phase 1 of this program, we are confident that we have the materials capability to meet the second phase goal (40 mW 30-60 GHz amplifier) had the program been continued.

o Processing Approach

Our approach to meet the FET and circuit fabrication goals of phase one, in addition to meeting the materials growth goals entailed using a hybrid e-beam/contact lithography fabrication process.

In this process sequence, quarters of 3" wafers are processed as described below using the e-beam machine for direct writig on the wafers for the first four levels:

1) "Fiducial" marks for establishing registration are written by e-beam in PMMA developed and ion milled. These milled "pits" are used for registration of subsequent e-beam levels.

2) Isolation Level: Mesas defining the active regions for FETs are exposed by e-beam. PMMA is used so the image is reversed by long UV exposure and developed. A wet etch is used to remove the thin active layers in the "field" regions where there are no FETs.

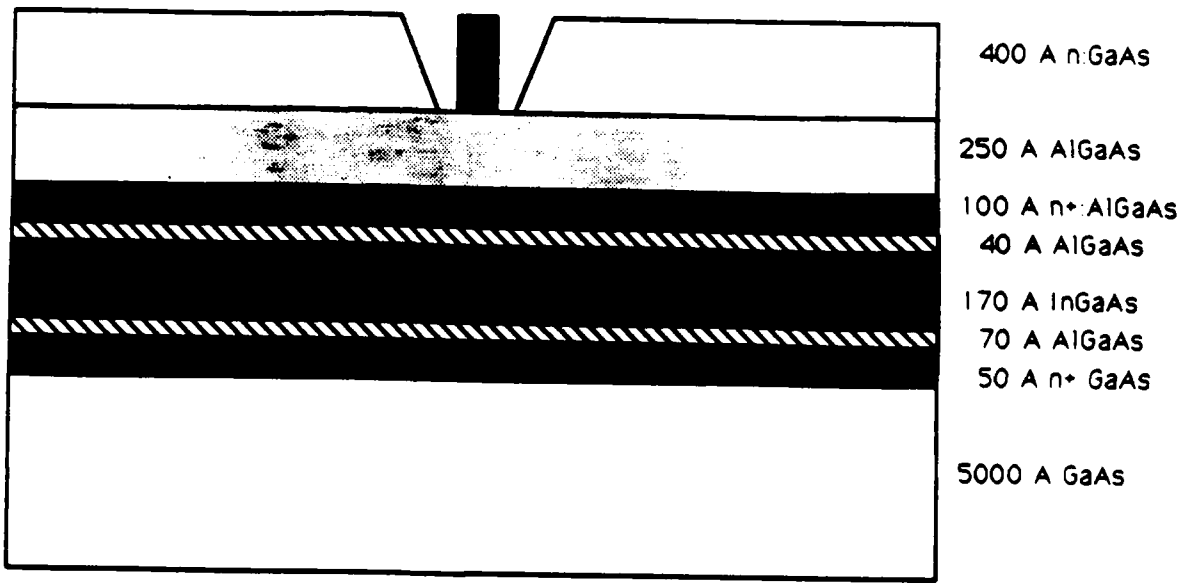


Fig. 11. Double heterostructure psuedo-pulse doped MODFET layer; channel current is improved by electron donation from both sides of the InGaAs channel.

3) Ohmic Level: Areas to have ohmic contacts are written by e-beam in a bilayer PMMA/PM(MA/AA) sandwich, which provides a liftoff profile after develop. AuGe/Ni is evaporated, lifted off and alloyed to produce ohmic contact to the mesas.

4) Gate Level: Quarter micron gate lines are written by e-beam in PMMA by alining (as for the above levels) to milled fiducial pits; development, recessing of the gate, gate metal evaporation and liftoff then complete the gate line definition.

5) Circuit Metal: A contact mask written at Honeywell with e-beam lithography are used with a chlorobenzene-leached photoresist to lift off circuit metal.

6) Capacitor/Passivation: SiN is deposited over the entire wafer quarter by plasma-enhanced CVD and is then patterned by a contact mask, written at honeywell and selectively removed everywhere except at metal-insulator - metal capacitors and over the source-drain region of passivated FETs.

7) Air-bridge Post Airbridge: Contact masks, again written by e-beam
8) are used to form airbridges and thick top (plated) metal interconnects. After the airbridge post level, a plating base is sputtered over the entire wafer and a second photoresist layer is used to mask an electroplated Au layer.

9) Wafer Thinning: Wafer quarters are lapped and polish to a full 100 μm thickness by mounting face down on substrate carriers.

10) Through-wafer vias selective backside metallization: wafer quarters
11) are patterned the backside for through-vias with an infrared contact aligner and the holes are etched with ion-beam assisted etching. Next, selective backside metal plating is done by using a photoresist layer to mask areas that are to be not plated. Both masks are written by e-beam.

The rationale for the choice of this process was that it was flexible, we had good experience with it for small circuit fabrication, and it used small MBE samples economically.

Good device characteristics were obtained with this fabrication process using material from growth runs 2 and 3. Fig. 12 illustrates dc FET characteristics obtained from wafer 877. These are also typical of FETs from wafer 878 and 879 and similar to FET results from wafers from growth run #3. Extrinsic dc transconductance exceeds 400 mS/m over a relatively large Vgs and Vds range and peak Ids exceeds 400mA/mm. On-wafer S-parameter data was obtained with Cascade Microtech Probe and $H_{21}(f)$ was calculated and extrapolated. Near the peak gm point f_T values were respectable for the MBE layer and fabrication process; SEM examination of the gate showed gate lengths near 0.34 μm rather than the target 0.25 μm. Fmax extrapolated from measured S-parameters was typically 120 GHz.

The equivalent circuit for a 50 μm FET was extracted from s-parameter data, optimized and entered into the monolithic 60 GHz gain all design file. See Section IV. The equivalent circuit predicted roughly 4.5 dB gain of 60 GHz, and slightly less than 60 GHz amplifier operation. The reason was due to a slightly larger Cgs in FETs on wafer 877 than in the model that had been used for circuit design. Gate and drain voltage variation in fT is plotted in Fig. 13. Two areas were identified for improvement: breakdown voltage of the FETs needed to be raised from 4.5-5.0 V observed to near 9V and the pinchoft and peak dc transconductance had to be broadened to allow larger gate voltage swing.

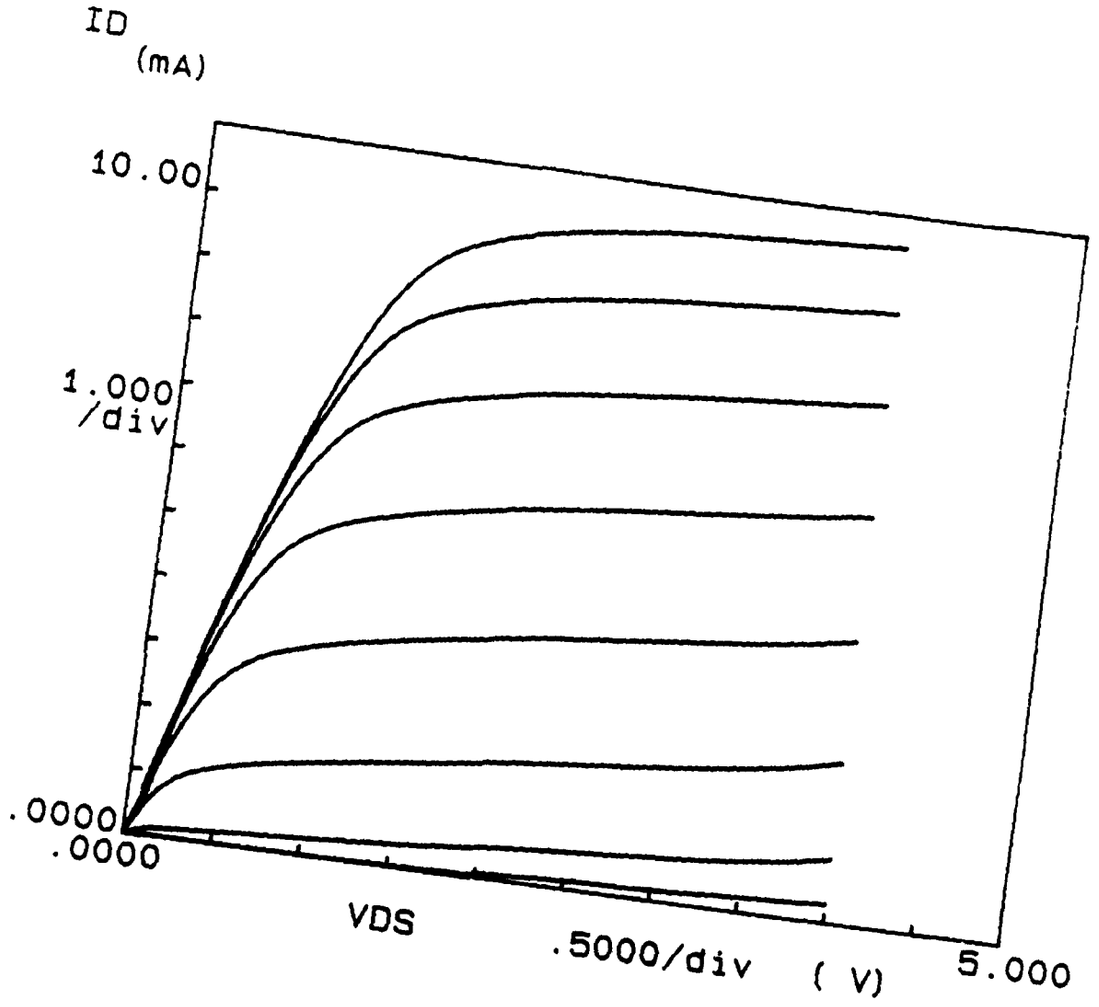


Fig. 12a. Drain characteristic of 25 μm MODFET V_{GS} is stepped (-0.4 to 1.0V).

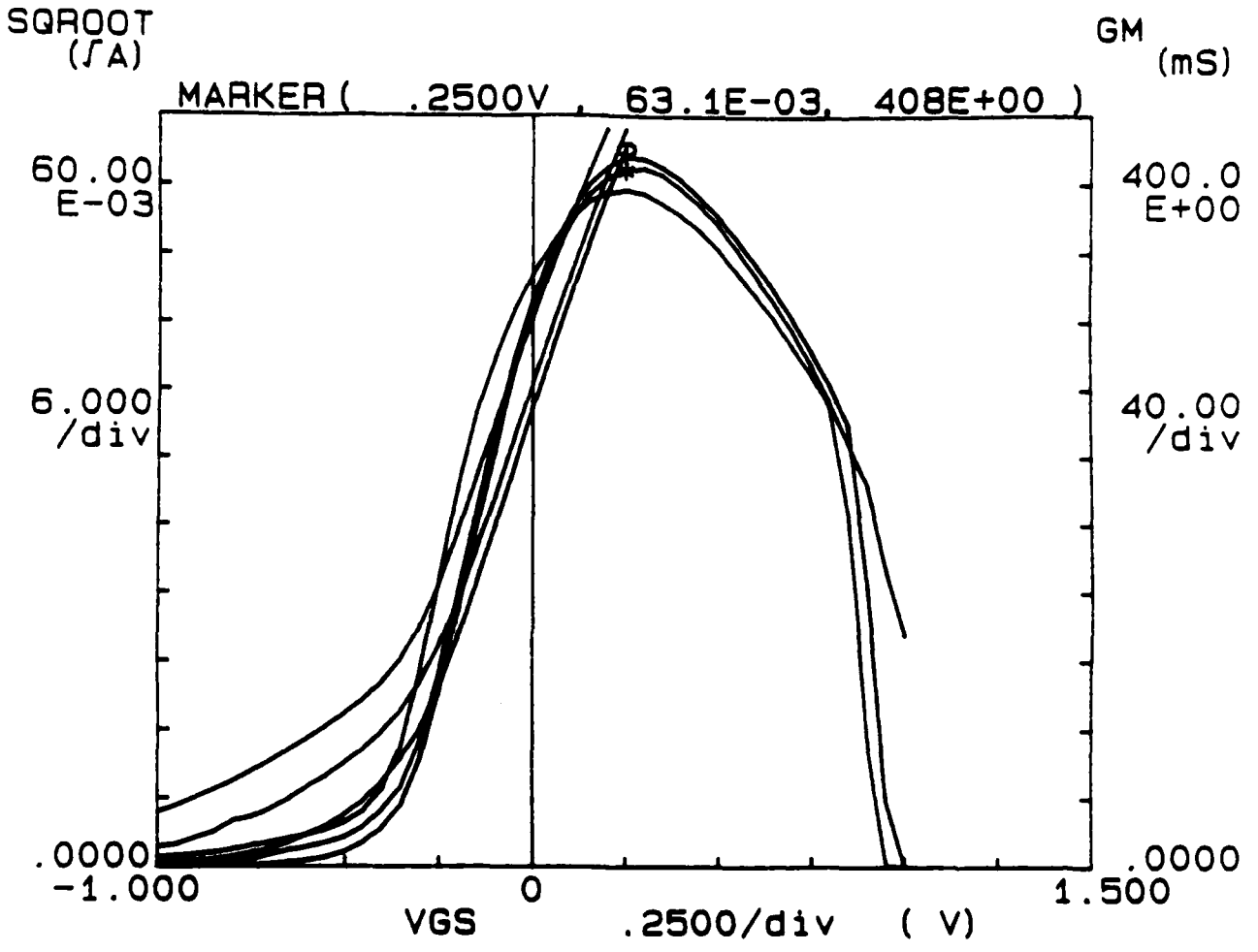


Fig. 12b. I_D and gm for 25 μm MODFET. The three curves are for V_{DS} = 2, 3, 4V.

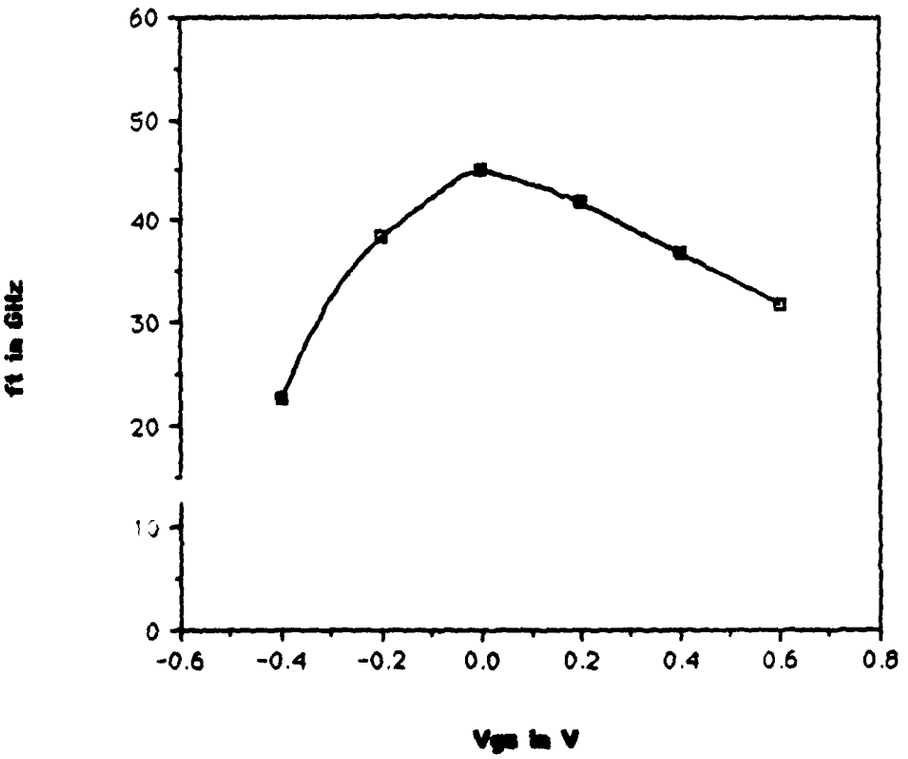


Fig. 13a. Vgs dependence of fT at V_{DS} = 2.5V

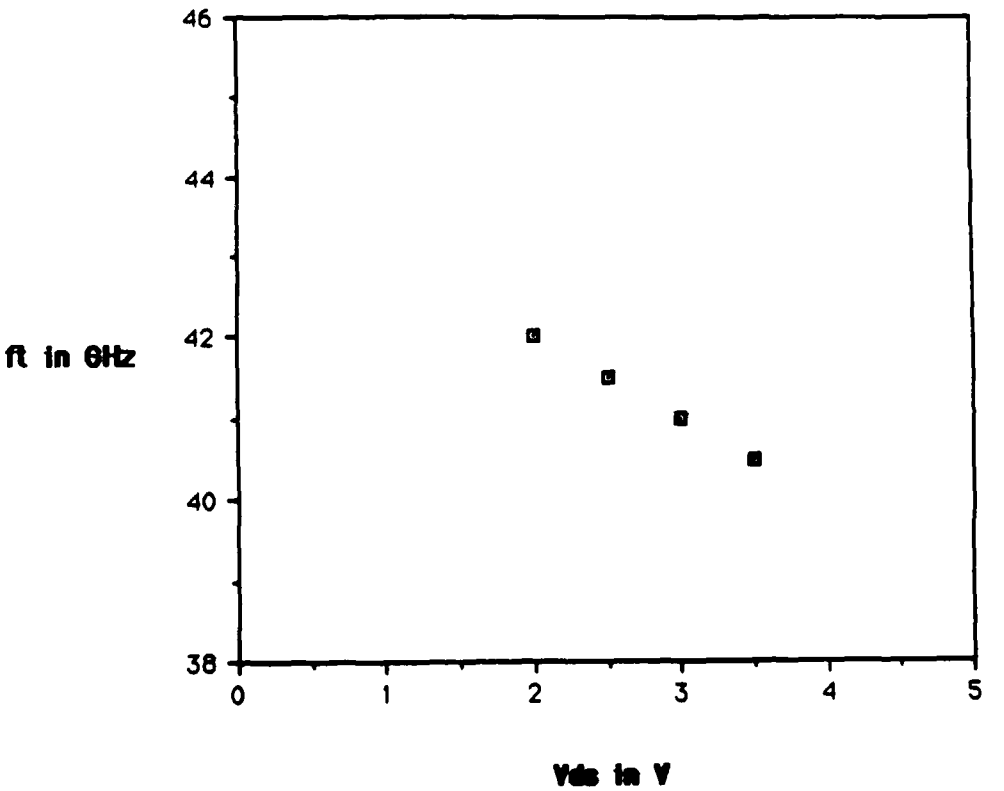


Fig. 13b. Vds variation of fT at Vgs = + 0.2V

Selected wafer quarters from the first fabrication run were thinned, backside metalized after frontside circuit metal was completed, and 60 GHz gain cells using 2 x 25 μm gate width FETs were tested. The phase-one goal of 10 mW output power at V-band was achieved on the first wafer quarters fabricated with a 50 μm gate width 60 GHz FET amplifier. Refer to Section IV for details.

Significant problems were faced in processing the large distributed amplifier circuits on the wafer quarters selected for completion of frontside and backside processing. A large run out error was seen in overlay of wafers produced with the hybrid e-beam/contact process. Isolation of the problem proved difficult because the electron-beam lithography tool (Cambridge 6.4) had just been relocated to our clean room from a nearby Honeywell location, where we had shared its operation personnel. Repeated hardware problems and problems with the compatibility of software upgrades caused very low uptime for a period of over 3 months. A detailed study of the run out problem showed that it was equally divided between mask fabrication run out and inaccurate fiducial placement for the starting fiducial level. Although techniques to reduce the run out were implemented we were unable to get registration for the 6 contact mask levels down to the level where we could reasonably expect yield of the large and complex 30-60 GHz distributed power amplifiers.

For the four reasons listed below, we concluded that our approach for fabrication of the large distributed power amplifiers for the proposed phase two would use optical projection stepper/e-beam lithography on full 3" MBE grown wafers. The motivation is higher yield and the specific reasons are listed below:

- While the e-beam/contact process used expensive e-beam write time for 4 levels, only gates would be written with the e-beam in the 3" process and the wafer stepper would do all others; a cost saving would result and process control effort with e-beam machine could be focused on maintaining the critical 0.25 μm gate dimension.

- The wafer stepper tool used local alignment and focusing, so run out is eliminated and typical level-to-level registration is 0.15 μm.

- Rather than fabricate nine 35$(mm)^2$ reticles, forty-one 70$(mm)^2$ reticles would be fabricated, providing a much larger number of reticles to yield working circuits.

- The e-beam/stepper process is the baseline 3" MESFET process at Honeywell and has benefited from a significant process development effort; some higher yield features includes implant isolation for a planar surface and RIE through-wafer vias.

To debug the 3" stepper/e-beam fabrication process prior to circuit fabrication in phase 2, three wafers from MBE growth run 4A were processed to FET level with an existing FET-only mask set. A

great deal was learned from these partially processed wafers and a number of growth process improvements were planned for later implantation. The wafers did not have n+ cap so the channel properties were apparent.

- o Wafer sheet resistance uniformity was adequate in the central 25 reticles but high at the wafer major flat and minor flat. See Fig. 14a. This pattern has been identified on other InGaAs channel wafers grown on 430. New growth will be planned to use the 425 to avoid the non-uniformity.

- o Wafer contact resistance uniformity (see Fig. 14b data in Ω mm) is good but some improvement in average value (0.184 Ω mm to 0.10 Ω-m) is required.

- o FET characteristics can be well reproduced across the 3" wafers.

The major conclusion of this de-bug fabrication run is encouraging: no serious problems would result from switching fabrication to a full 3" stepper/e-beam process and significant improvements in circuit number and yield would result. Our approach for phase two and subsequent phases would, had the program been continued, appear correct.

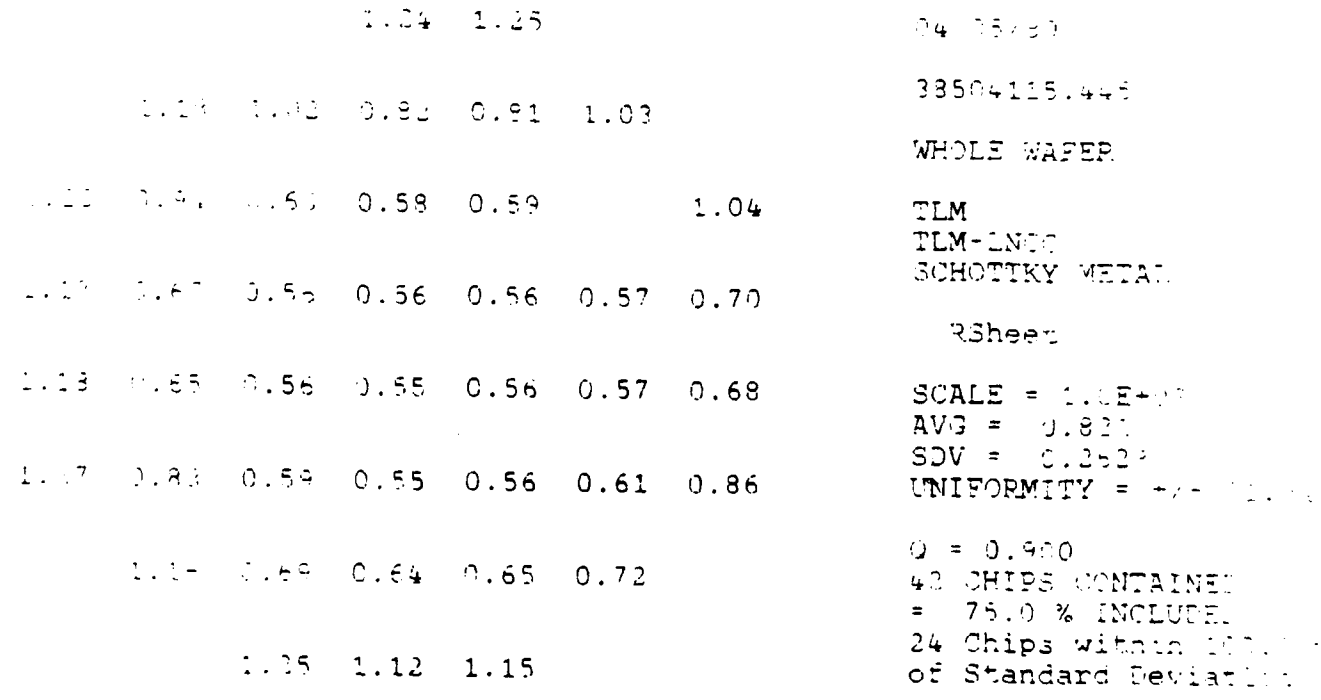


Fig. 14a. Sheet resistance (channel) uniformity of a 3" InGaAs MODFET wafer; units are Ω/□.

			3.11	3.01			34.05 [illegible]
							3850+1[illegible].+-5
	0.99	3.[illegible]	[illegible].83	3.09	2.74		
							WHOLE WAFER
2.79	2.43	3.15	2.95	2.29		0.56	TLM
							TLM-LN[illegible]
							SCHOTTKY METAL
1.11	2.38	3.00	2.46	2.09	1.90	2.52	
							R1
1.03	1.93	3.20	2.22	1.85	2.09	2.36	SCALE = 1.05[illegible]1
							AVG = 1.840
							SDV = 0.0475
[illegible].06	0.55	1.94	2.37	2.18	1.92	1.20	UNIFORMITY = +/- [illegible].9%
							[illegible] = 0.900
	0.58	1.23	2.18	2.13	1.08		42 CHIPS CONTAINED
							= 75.0 % INCLUDED
							28 Chips within [illegible]
		0.20	-0.33	0.00			of Standard Deviation

Fig. 14b. Contact resistance in Ω-mm for a 3" InGaAs channel MODFET wafer.

IV. 60 GHz Gain Cell Development

Our 60 GHz "gain cells" essentially consisted of discrete devices and monolithic single-stage amplifiers obtained from the first mask set. Two such monolithic amplifiers were delivered to ONR, one of which was mounted in a waveguide test fixture. Discrete device testing made use of a waveguide test fixture employing e-plane probes, while the 60 GHz monolithic amplifier testing was accomplished using an in-line waveguide fixture incorporating antipodal waveguide-to-microstrip transitions. Design data was obtained from equivalent circuits derived from microwave s-parameter measurement. In conjunction with the narrow-band test fixtures a broadband test fixture design for mm-wave octave-bandwidth MMIC testing was also completed.

o RF Characterization of 60 GHz Hybrid Amplifier

Figure 15 shows the .25 x 50 microns gate width HEMT equivalent circuit derived from the measurement of on-wafer S-parameters of ONR-2 #879 wafer. The layout of the device is shown in Figure 16. Input and output matching circuits for the amplifier were designed on a 4 mils thick quartz substrate. Quarter wave transformers that transforms from 50 ohms to 15 ohms impedance were used to match the input and the output of the amplifier. A biasing filter was also included on the quartz substrate. For the test fixture, a V-band E-plane-probe transition test fixture was used as shown in Figure 17. Two micrometers are used to accurately and reproducibly adjust the location of the waveguide backshorts. The microstrip-probe circuits are fabricated on 5 mil thick cuflon substrates. An insertion loss of 1.5 dB and return loss of about 20 dB is obtained from 56 to 65 GHz for two back-to-back transitions (Fig. 18). With 200 mils of 50 Ω "thru line" the total insertion loss is the range of 2.5 to 3 dB over this band. The amplifier input/output matching circuits were mounted with indium solder of 149^{0}C and connected to the microstrip probe transitions with mesh wire. A length of 5.5 mils gold wire for the gate and a 12 mils long for the drain was used to connect the amplifier to the input and output microstrip matching circuits. At V_D = 4.3V, I_D = 10.5 ma and V_G = .05V the small signal response is shown in Figure 19. After acounting for 2.5 dB fixture loss, a gain of 5.1 dB was obtained at 59 GHz. Power measurement indicated a saturated output power of 6-10 mW. Similar results were obtained on several other 0.25 x 50 micron devices. An amplifier with device gate periphery of 0.25 x 100 micron was also assembled and its small signal performance is shown in Figure 20. Power measurements performed on this device did not yield higher power as compared to the 50 micron devices. We believe, the added parasitics associated with the larger gatewidth device and the bonding wire inductances associated with the hybrid amplifier assembly prevented the realization of greater output power with the larger gatewidth FET.

o Monolithic 60 GHz Amplifier Characterization

The 60 GHz single-stage amplifiers were designed on the basis of conjugate impedance matching at input and output. Figure 21 shows the CALMA layout of this reactively matched amplifier. Sections of high

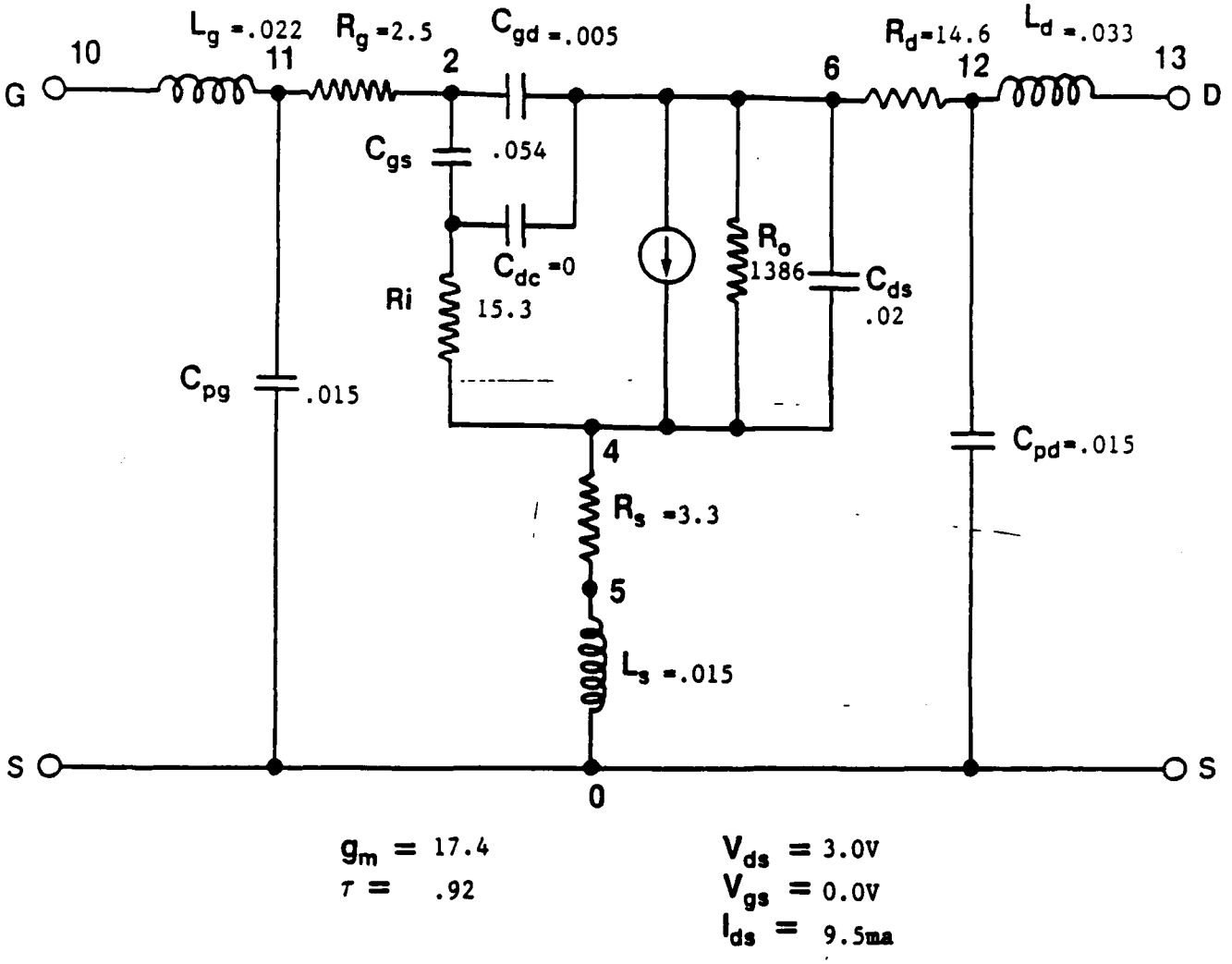


Fig. 15. Equivalent circuit model for 0.25 x 50 micron HEMT, wafer ONR-2 #879.

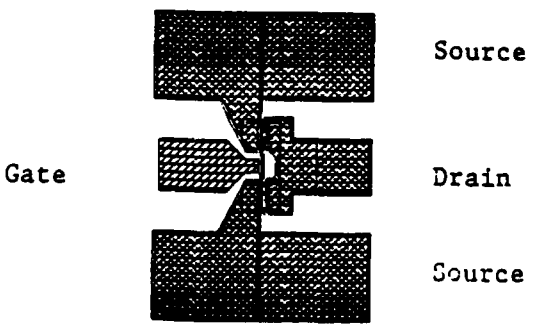


Fig. 16. Overall geometry for 0.25 x 50 microns HEMT device.

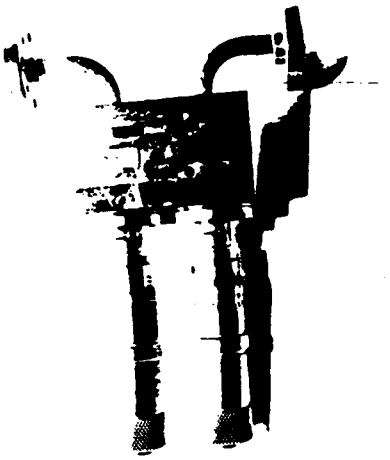


Fig. 17. V-Band E-Plane microstrip probe transition test fixture.

impedance microstrip lines are used for impedance matching on the RF input and output lines, while radial open stubs centered at 60 GHz are used to present a low impedance (virtual ground) to the 50 micron MODFET source pads. With this approach, the dc ground is achieved with bond wires placed as near the apex of the radial stub as can be managed.

The 60 GHz monolithic amplifiers were fabricated on the MBE material from growth runs #'s 2 and 3. This material employed an InGaAs/GaAs psuedomorphic structure and did not incorporate the pulse doped features of later material growth runs. Furthermore, due to prblems with the e-beam lithography FETs having 0.34 micron gates instead of the nominal 0.25 micron gate lengths were fabricated. The resultant devices had maximum transconductances of 400 mS/mm, ft's of 40 GHz and fmax's of over 100 GHz (the 1st two figures of merit were calculated from s-parameter measurements).

The 60 GHz monolithic chips were assembled in our in-line test fixtures employing antipodal fin-line waveguide to microstrip transitions. The "thru" insertion loss of these fixtures is about 1.5 dB at 60 GHz. Figure 22 shows typical RF results obtained on our monolithic single stage amplifier. A small signal gain of 4 dB is obtained at 58 GHz with a 3 dB bandwidth exceeding 5 GHz. Power measurements were also made on these amplifiers. Figure 23 shows the result of greater than 12 mW of output power at 60 GHz. However, additional tuning of the input and output circuits had to be used to achieve this power output level. Note that due to this large signal tuning the small signal gain was reduced to 2.9 dB. The 1 dB gain compression point is at 9 mW output power.

To fulfill the contract deliverables, two such amplifier "gain cells" and one test fixture were delivered to ONR.

o Broadband Test Fixture Design

The objective of this work was to develop a test fixture for the broadband (30.5 to 61 GHz) amplifiers being developed.

Development of the test fixture included the evaluation of three different transmission line transition approaches: coax to microstrip transition, finline waveguide to microstrip transition, and ridge waveguide to microstrip transition.

<u>Coax to Microstrip Transitions:</u>

The coax to microstrip approach is the most viable of the three transitions. There are two different alternatives being pursued in industry at the present time.

The first connector is a DC to 60 GHz, 1.65 mm coaxial Teflon dielectric connector being developed by Dynaware Inc. The advantage of this connector is that it employs a solid dielectric. That promises to make it more rugged and durable. However, there are several disadvantages to

this connector. First, this connector is still in the development stage and is not yet in the commercial market. Second, the required adapters needed to interface with this connector type are yet to be designed and then developed.

The second connector that will suit our needs is a 1.8 mm air dielectric coaxial connector that Wiltron is currently marketing as a "V" connector. Its usable range is from DC to 65 GHz. This connector is already a catalog item for Wiltron. The "V" connector will mate with the 2.4 mm connector which means it is compatible with some commercially available test equipment (CTE). Wiltron also has a line of the necessary adaptors for the "V" connector to allow the use of waveguide or coaxial CTE. Hewlett-Packard is also working on a similar connector that may be compatible with the "V" connector.

The "V" connector is the coaxial style used in the test fixture shown in Figure 24.

Waveguide to Microstrip Transisions:

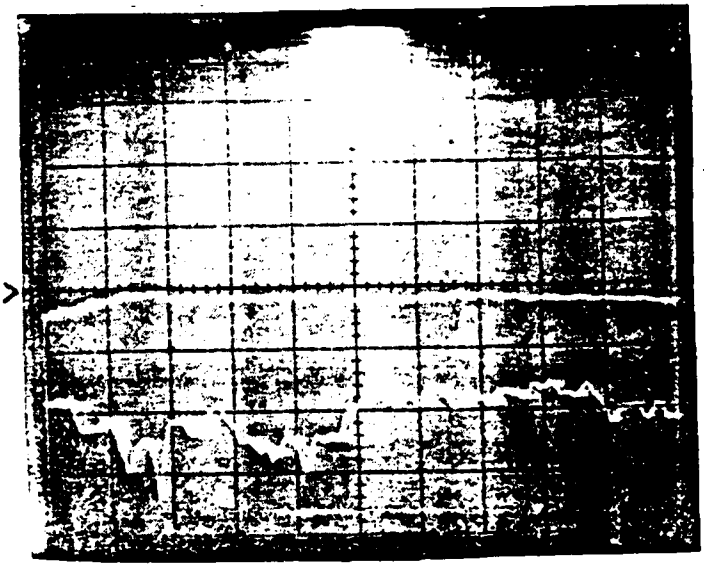
The waveguide to microstrip transition is a less preferred approach. This approach would require further development to establish a transition that would match the performance of the coaxial design. Two alternatives were considered: finline waveguide to microstrip, and ridged waveguide to microstrip.

The waveguide finline to microstrip was not pursued. It was concluded that a finline transition from 30-60 GHz would be very difficult at best, given the wide bandwidth and the frequency of interest. This transition approach was then abandoned.

The ridged waveguide showed more promise. In order to optimize the transition, a multi-stage impedance transition was modeled using the techniques presented by Cohn[5]. An impedance transition could be used that had the proper bandwidth and excellent simulated performance (Figure 25).

The physical realization was then attempted using the design equations by Hoefer and Burton[6] for ridged waveguide. The problem with this transition type is in the physical realization of the proper ridged waveguide characteristic impedance. In order for the transition to operate over the wider bandwidth and still maintain reasonable operating parameters the transition needs to use more impedance transforming stages. More stages mean more difficulty in fabrication, more insertion loss, and more chance of inaccuracies occurring to decrease the performance of the entire system.

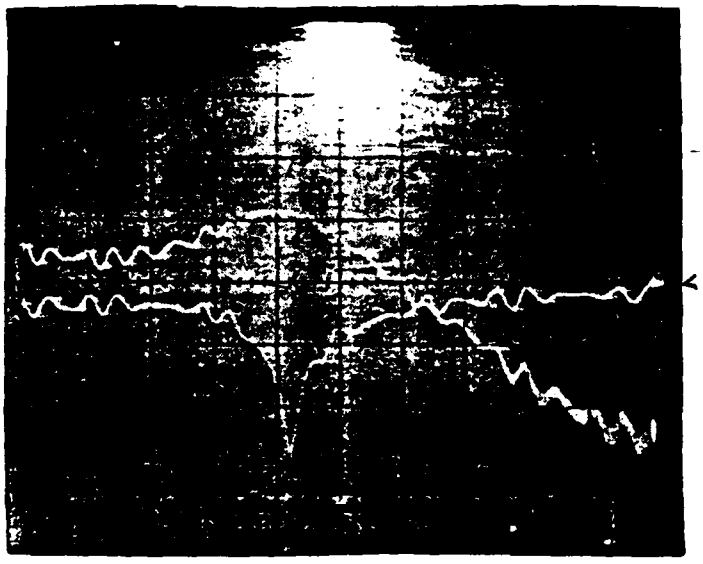
The ridged waveguide may still be a viable approach if desired, but a much larger effort would have to be expended. Several engineering models would have to be built and tested before a transition of this type would be perfected.



Vert: 5dB/div (IL)
10 dB/div. (RL)

Horiz: 55-65 GHz

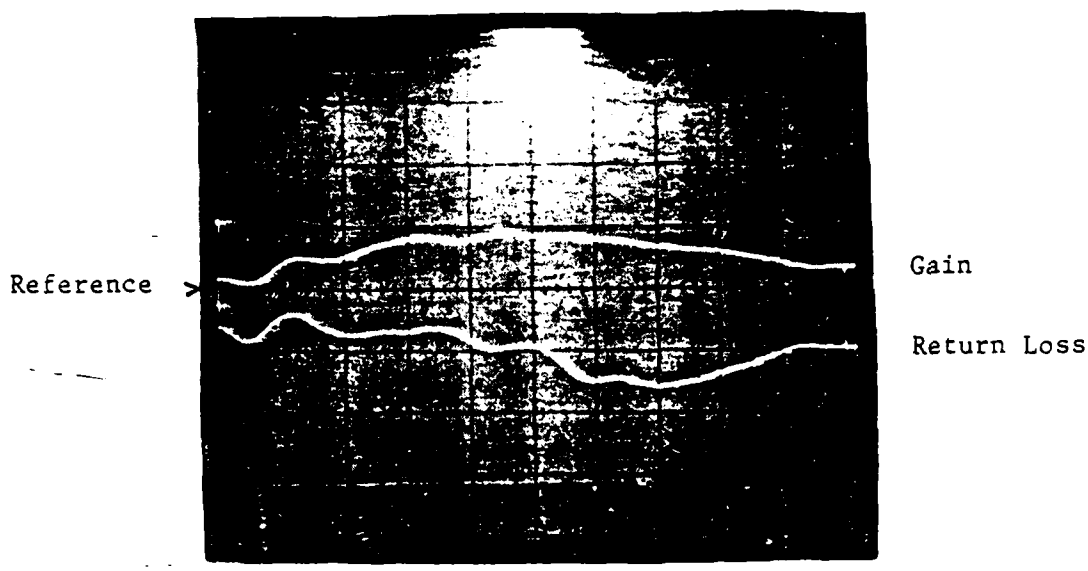
Fig. 18. RF performance of V-band test fixture using waveguide to 5 mil Cuflon E-field-probe transitions.



Vert: 5 dB/div. (Gain)
10 dB/div. (RL)

Horiz: 55-65 GHz

Fig. 19. Gain response and input return loss of 50 micron HEMT amplifiers from wafer ONR-2 #879 (device #1).



Vert: 5 dB/div. (Gain)
10 dB/div. (RL)

Horiz: 55-58 GHz

Fig. 20. Gain response and input return loss of 0.25 x 100 micron HEMT amplifier.

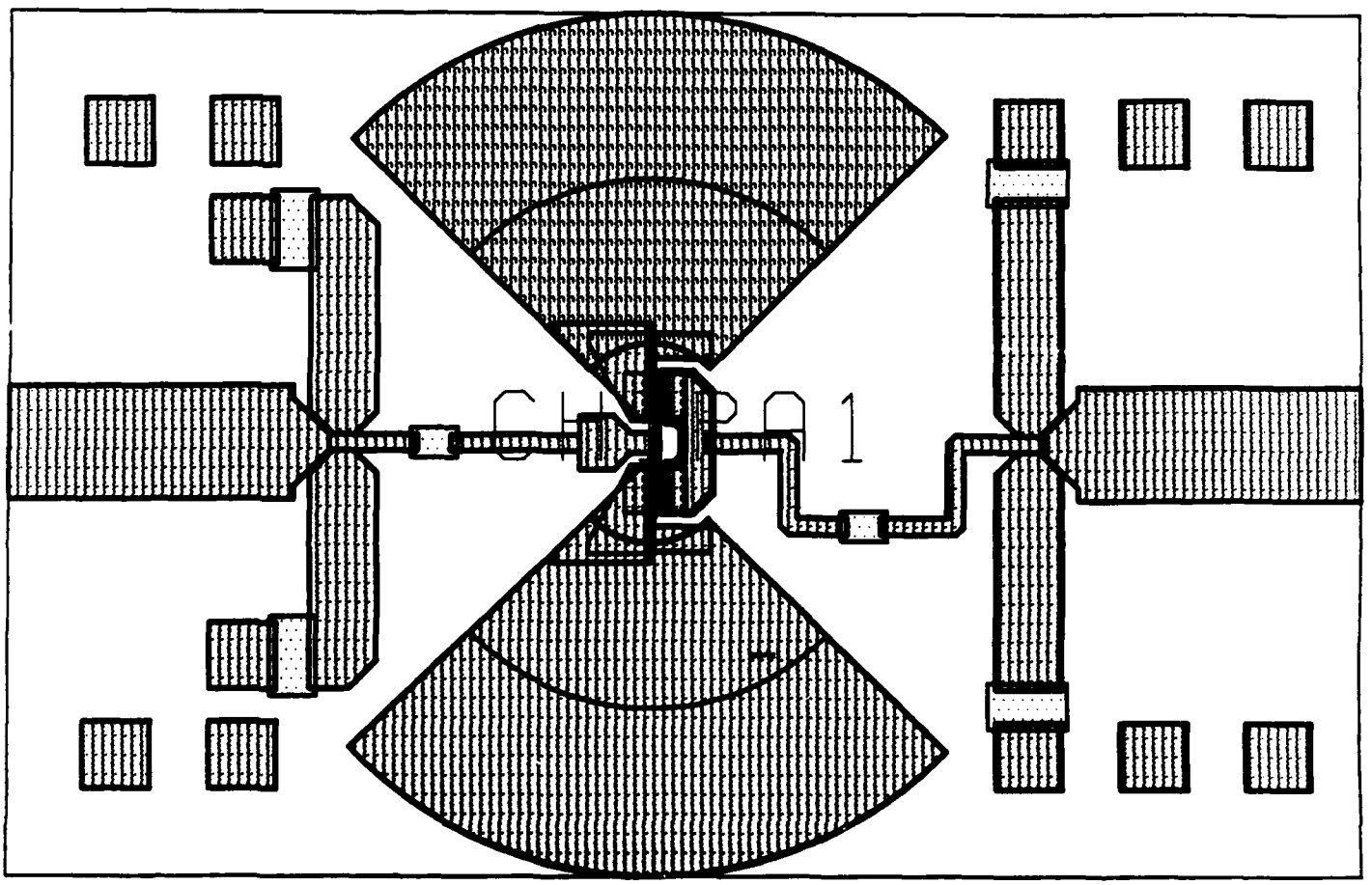
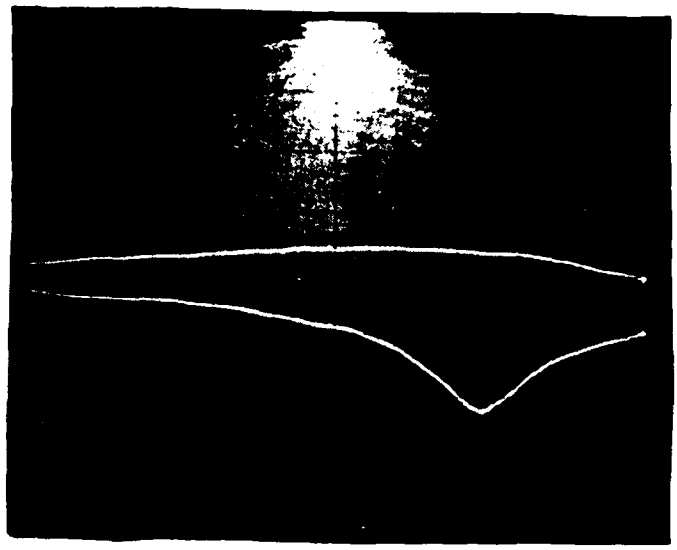
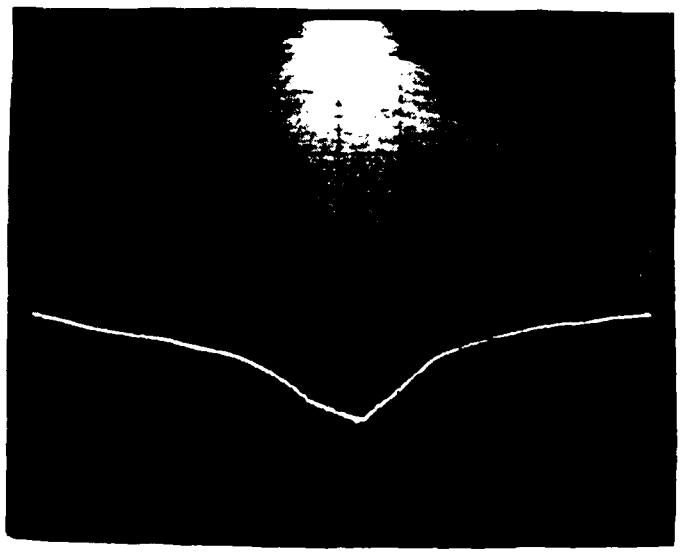


Fig. 21. Reactively matched 60 GHz amplifier with radial stub source ground.



Horz: 55-60 GHz



Vert: 5 dB/div. (Gain
10 dB/div. (RL)

Fig. 22. RF Results: ONR 60 GHz MMIC Amplifier 0.4 μm x 50 μm Gate.

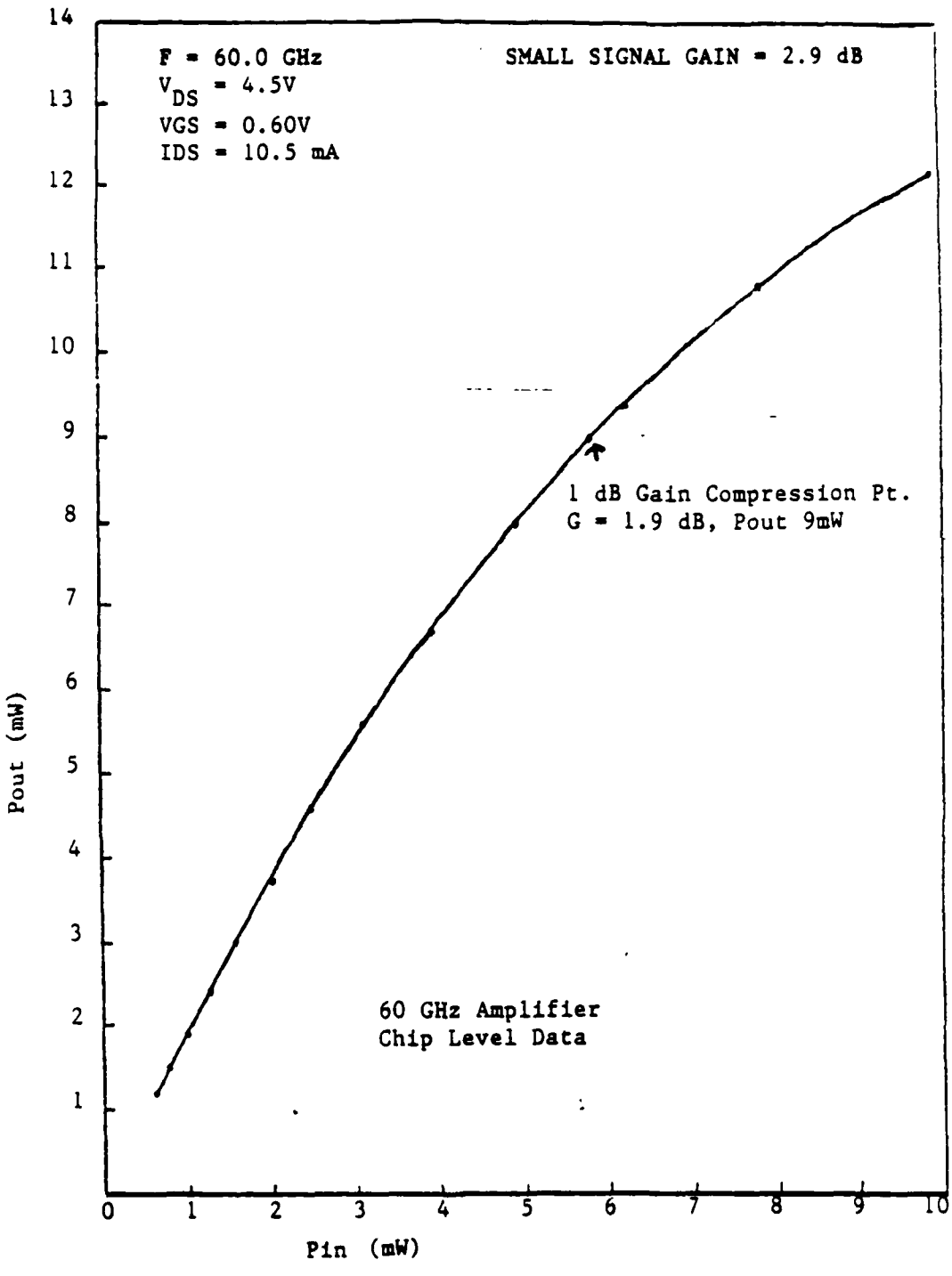


Fig. 23. Gain compression characteristics for a modified* 60 GHz amplifier chip.
*Input and output circuits were tuned to 60 GHz for testing purposes.

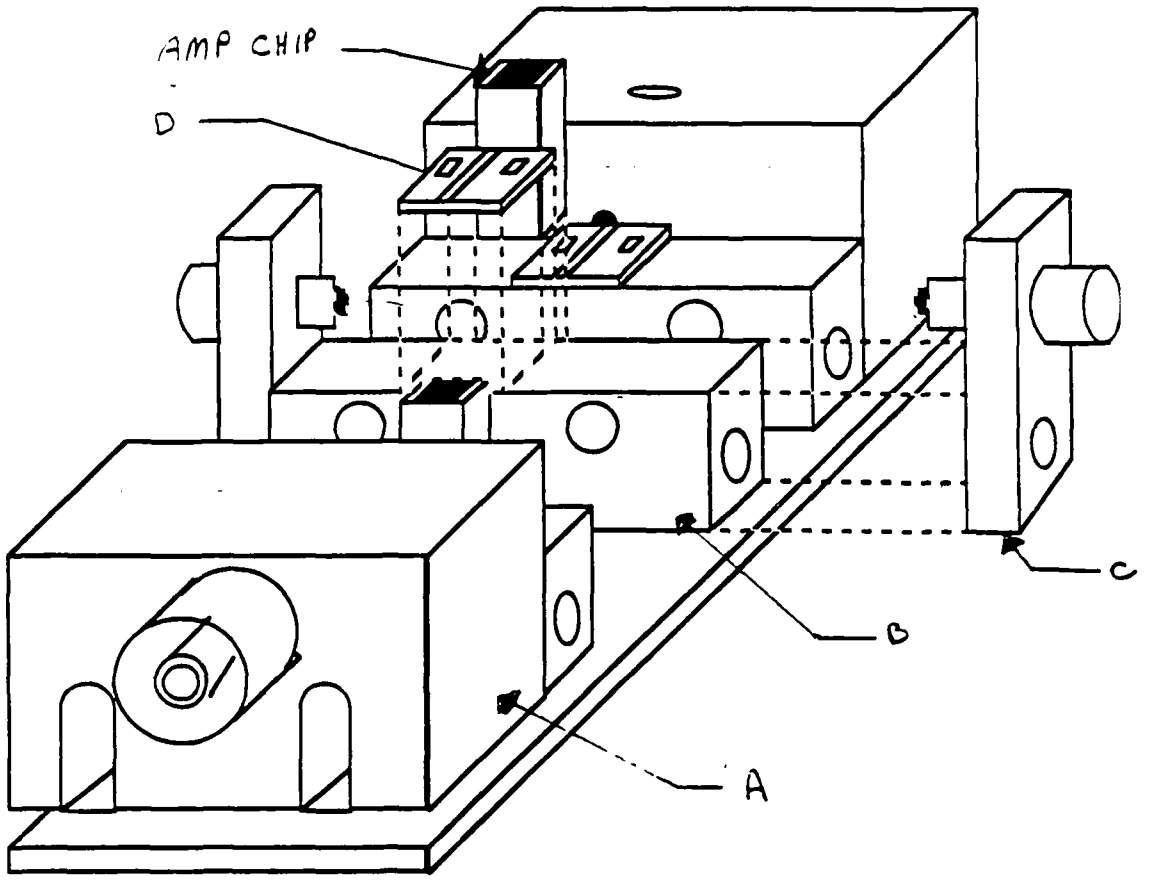
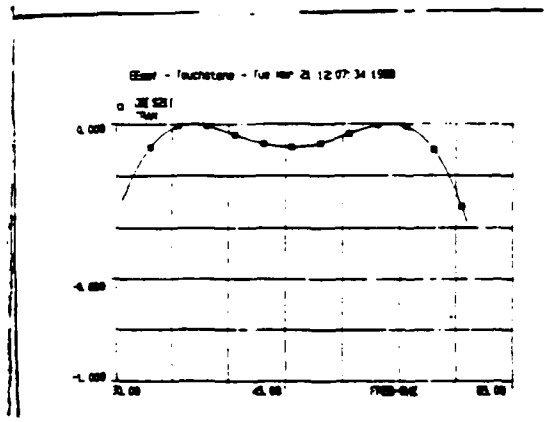


Fig. 24. Coax test fixture. A layout drawing (mechanical drawings were also completed) of the suggested test fixture configuration. Two amplifier chips under test are in the fixture.



INSERTION LOSS

RETURN LOSS

Figure 25. 4 Stage Impedance Transition

V. Conclusions

The objective of this program was to begin the development of a class of highly efficient, wideband, easily cascadable, mm-wave (e.g., 30-60 GHz) monolithic amplifiers with power output capability approaching 1W. This technology would have application to a wide variety of EW systems requiring high power, high efficiency, broad bandwidth and small size. The program was planned as a multi-phased effort and with a duration of at least five years. Much of the work accomplished during the first two years formed the basis for the longer term objectives. Unfortunately, funding for later phases was not available and the program was concluded at the end of the first two years. Several important findings, however, were determined during these first two years. These are summarized below.

To achieve reasonable gains and performances for the broadband MMICs considered in this program, advanced MODFET devices using strained layer (psuedomorphic) InGaAs channel MBE material were developed. Combined with 0.25 micron lithography, such devices were demonstrated to have gains of at least 4 dB at 60 GHz. However, large signal operation revealed power output limitation to about 0.2W/mm for 50 micron gatewidth devices. Larger gate widths, e.g., 100 microns, did not improve the output power and indeed yielded a power density of less than 0.2W/mm. The former limitation is primarily due to low (3 to 4V) breakdown voltage at the drain, while the latter problem is primarily due to increased reactive parasitics associated with the hybrid circuit mounting and layout of the 100 micron gate width MODFETs. To correct these problems, we introduced a pulse-doped structure in the psuedomorphic materials structure to increase breakdown voltage, and focused our circuits designs on the use of 50 micron devices. Three-inch MBE wafers using the pulse-doped structure were grown (with sheet carrier density of $n_s = 4\ 10^{12}$ cm^{-2} and room temperature monolithics of $\mu = 4100$ cm^2/Vs) and prepared for use in the second phase of the program on the new mask set design.

Although our first mask set contained a variety of monolithic circuits including a first-pass design of a 30-60 GHz distributed amplifier, low processing yield, especially on the more complex and dense layouts prevented the testing of many of these designs. Primary cause for the low yield was the inadequacy of the hybrid optical-contact/e-beam lithography approach in terms of mask alignment error. To remedy this situation, all our circuits were translated to our 3-inch 10:1 optical projection/e-beam lithography process, wherein local alignment on each of the 50 reticles on a 3-inch wafer is accomplished by the CENSOR optical projection aligner. We believe such an approach is essential for realizing high yield on complex large area MMICs such as the distributed amplifiers required for this program. It was planned to begin the fabrication of the new mask set once we had the "go-ahead" for phase II.

Despite the above problems, we satisfied the contract requirement for phase I with the delivery of 60 GHz "gain cells". These monolithic 60

GHz single stage amplifiers were one of the first such circuits developed in the industry, especially in light of the fact that the MMICs were fabricated on 3-inch psuedomorphic InGaAs channel material.
In parallel with the basic materials and device development, a comprehensive advanced design and study phase which included analytical as well as experimental work was conducted at the University of Wisconsin. Several important results were achieved including novel distributed amplifier designs applicable to high power, high gain, and high efficiency operation at mm-wave frequencies.

An initial design of a 30-60 GHz distributed amplifier using available equivalent circuit data from our first psuedomorphic MODFET devices was completed and included on our first mask. These devices had cut-off frequencies (fmax) of about 120 GHz. The predicted distributed amplifier response was on the order of 4 to 5 dB small signal gain across the band. To increase the gain and power performance negative resistance compensation on the gate line was investigated. Combined with a cascode FET for the elemental gain cell the negative resistance gate line loading and the reduced drain line attenuation provided by the cascode devices revealed significant improvement in the gain bandwidth performance of the distributed amplifiers. Practical circuit topologies including bias distribution were worked out for these cases. The cascode circuit, although allowing higher small signal gain, does not offer increased power capability. Studies revealed that the second, common gate FET of the cascode connection, is subject to high voltage swing operation and breakdown occurs at comparable output power levels as that experienced by a single gate distributed amplifiers.

An important new circuit topology for a band-pass distributed amplifier was also developed. To increase the gain at mm-wave frequencies a band-pass topology allows optimizing the gain in the band of interest, rather than distributing the gain from DC to the highest frequency of interest as is the case in the conventional low-pass distributed amplifier topology. Several design cases revealed that negative resistance compensation is especially significant for the band-pass topology to reduce excessive gate line attenuation at mm-wave frequencies. This topology shows promise for development of broadband DA's having octave bandwidths with center frequencies approaching 100 GHz.

Class B operation was investigated for high efficiency operation. Although drain efficiencies of up to 69% were experimentally demonstrated, operation in Class B places even higher demands on device characteristics. High breakdown voltages, and "hard" pinch-off characteristics with high transconductance at low current levels is essential before the potential benefits of Class B operation can be exploited especially for distributed amplifiers. Several test circuits were designed to begin a systematic study of the practicality of Class B operation for DAs. From a device point of view, the psuedomorphic InGaAs channel MODFETs with pulse-doping in the charge supplying layer may be best suited for operation in Class B regime.

VI. Recommendation for Future Work

As outlined in our original proposal future work should follow Phase II efforts and concentrate on fabrication of the 30-60 GHz DA using pulse doped psuedomorphic InGaAs channel MBE materials. For good yield, a hybrid optical projection/e-beam lithography approach is recommended. Along with these mm-wave circuits fabrication and evaluation of the various test circuits should be completed to establish the viability and data base for design of Class B DA's.

We believe the encouraging results obtained on the analysis of advanced DA designs warrants initial fabrication and realization of these MMICs. Monolithic realization of negative resistance compensated and compensated cascode DA's is recommended. For high frequency DA's where gain is required over a specified band (rather than from DC to some cut-off frequency) the monolithic realization of a DA based on a band-pass topology (preferably with gate line compensation) is recommended, especially for center frequencies approaching 100 GHz. Finally, work that was initiated under Phase I for the development of travelling wave FET amplifier (TWF) should continue to be studied including a cascode version of a TWF.

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APPENDIX

Attenuation Compensation in Distributed Amplifier Design

STEVE DEIBELE, MEMBER, IEEE, AND JAMES B. BEYER, SENIOR MEMBER, IEEE

Abstract—A high-gain common-gate FET can present at its drain a broad-band impedance characterized by a (frequency-dependent) negative resistance and a capacitance. This is examined both theoretically and experimentally. Loading the input and/or the output lines of a distributed amplifier with this circuit reduces the signal losses, leading to an increase in the allowed number of active devices with a consequent increase in the gain–bandwidth and gain–maximum frequency products. The cascode circuit, a related loss reduction network, is also evaluated because of its use in distributed amplifiers. Several designs employing the common-gate FET loss-compensating circuit and/or the cascode amplifying circuit are compared to a conventional distributed amplifier optimized for gain–bandwidth product. Simulated gain–maximum operating frequency product increases of 27 to 245 percent over that of the optimized conventional distributed amplifier are shown. The increase in single-stage amplifier gain provided by this technique often results in (proportionally) higher maximum output power.

I. Introduction

IMPROVEMENT in the gains, power outputs, and bandwidths of recent monolithic distributed amplifiers (DA's) [1]–[11] has been prevented by three factors: the input line attenuation, the output line attenuation, and the dynamic (linear) range of the input signal. The primary loss mechanisms of the two lines are the transistor loadings rather than the (microstrip) interconnecting line losses. Thus, all three performance-limiting factors may be addressed by careful transistor design. Advanced transistor design is important for DA improvement, but is not the only means available.

This paper reports on a novel "negative resistance" (NR) circuit which lessens the line attenuations and can lead to increases in the amplifier gain–bandwidth, gain–maximum frequency, and power–frequency products. The cascode circuit, related to the NR circuit, is also discussed. An approximate stability analysis of the (four-port) DA is presented. Lastly, the enhanced performance promised by the NR circuit is indicated.

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II. Conventional Distributed Amplifier Analysis

A typical conventional DA circuit consists of periodically spaced field-effect transistors (FET's) which are interconnected by electrically short, high-impedance microstrip lines [12]. A DA design may be qualitatively described as a set of artificial input and output lines coupled by (FET) transconductances.

In this paper "conventional" refers to those DA's for which the amplifying element is a common-source FET and for which no active circuit loss compensation is used. All other DA's are said to be "unconventional" or "modified."

Analytical studies of a simplified conventional DA have been completed, yielding insight into design fundamentals and trade-offs [12]–[14]. One important conclusion is that the line attenuation parameters A_g and A_d control the gain and bandwidth. Highlights of the analyses follow below.

The simplified transistor equivalent circuit (shown in Fig. 1) applied to the DA circuit of the above studies results in the following gain and attenuation expressions:

$$A = \frac{g_m\sqrt{R_{01}R_{02}}\cdot\sinh\left[n(A_g - A_d)/2\right]\exp\left[-n(A_g - A_d)/2\right]}{2\sqrt{1+(X_k)^2\left[\frac{\omega_c}{\omega_g}\right]^2\sqrt{1-(X_k)^2}}\sinh\left[(A_g - A_d)/2\right]} \quad (1)$$

$$A_g = \frac{(\omega_c/\omega_g)\cdot(X_k)^2}{\sqrt{1-\left[1-\left[\omega_c/\omega_g\right]^2\right]\cdot(X_k)^2}} \quad \text{(nepers/section)} \quad (2)$$

$$A_d = \frac{\omega_d/\omega_c}{\sqrt{1-(X_k)^2}} \quad \text{(nepers/section)} \quad (3)$$

where $\omega_g = 1/(R_gC_{gs})$, $\omega_c = 2/\sqrt{L_gC_{gs}} = 2/\sqrt{L_dC_{ds}}$, $\omega_d = 1/(R_{ds}C_{ds})$, $X_k = \omega/\omega_c$, $R_{01} = \sqrt{L_g/C_{gs}}$, and $R_{02} = \sqrt{L_d/C_{ds}}$. The variable A represents the amplifier voltage gain per stage. The variables A_g and A_d are the input line and output line attenuation terms, respectively. Physically, R_{01} and R_{02} represent the low-frequency input and output line image impedances. The term X_k is a frequency normalized to the LC structure cutoff frequency. Lastly,

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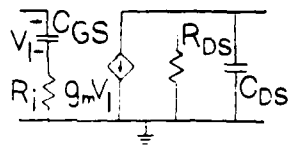

Fig. 1. Simplified common-source FET equivalent circuit.

ω_g and ω_d are the FET input and output impedance corner frequencies, respectively.

From (2) and (3), one notes that A_d is frequency invariant until nearing the LC cutoff frequency ($X_k = 1$), whereas A_g varies approximately with the square of frequency. Thus, at low frequencies A_d dominates the DA response while A_g begins to play a role at midband. The dc gain expression given below in (4), derived from (1)–(3), shows the performance limitations imposed by A_d:

$$\text{dc gain} = A_0 = \frac{g_m \sqrt{R_{01} R_{02}} \left[1 - \exp\{-nA_d(0\text{ Hz})\}\right]}{4 \sinh\left[A_d(0\text{ Hz})/2\right]}$$

$$= A_0(n). \tag{4}$$

The maximum dc gain is inversely proportional to $\sinh[A_d(0\text{ Hz})/2]$. Lower output loss FET's, higher image impedances, and/or higher gain FET's are necessary to extend the dc gain limits in the conventional DA. At high frequencies, the impact of the input line attenuation term A_g is felt. Reduction of A_g allows higher DA operation frequencies. Equations (1)–(4) indicate several design trade-offs which have been addressed in the literature.

III. Negative Resistance Loss Compensation

Examinations of (1) indicate DA gain improvement with decreasing section attenuation factors A_g and A_d. "Active" impedances placed along the loaded lines can lessen or overcome the attenuation (see Appendix, Fig. 11). Active impedances, characterized by frequency-dependent reactances and negative resistances, reduce the net attenuation terms by compensating the signal losses dominated by the positive transistor resistances R_i and R_{ds}. Thus "negative resistance (NR) compensation" aptly describes the concept.

The impact of NR compensation is twofold. First, by lessening the attenuation on one or both of the lines, more sections can be usefully added to a single DA stage. The increased single-stage gain permits a proportional maximum output power increase in those amplifiers limited by the dynamic (linear) range of the input signal. The maximum amplifier output power is then given by $G_p \cdot P_{in(\max)}$, which is proportional to the single-stage amplifier power gain G_p and to the (limited) maximum input signal strength $P_{in(\max)}$. The second impact of NR loss compensation is an extension of the bandwidth. Broad-band loss compensation on either DA line permits significant bandwidth increases.

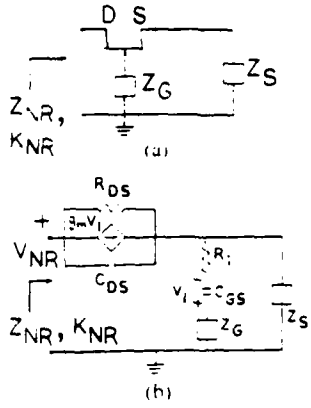

Fig. 2. A common-gate FET circuit including impedances Z_G and Z_S both encountered in the FET biasing circuit. (a) Circuit schematic. (b) Simplified equivalent circuit.

IV. The Common Gate Negative Resistance Circuit

The schematic and the simplified circuit model of a type of common-gate FET circuit are found in Fig. 2. When driven at its drain terminal, such a circuit can provide a negative resistance and a capacitance over a wide band of frequencies. Loading the artificial transmission lines of a DA with this circuit results in a considerable reduction in attenuation with minimal dispersion. Equation (5) shows the resulting input impedance, Z_{nr}:

$$Z_{nr} = \frac{R_{ds}}{1 + j\omega C_{ds} R_{ds}} \left[1 + \frac{g_m Z_s}{1 + j\omega C_{gs}(R_i + Z_s + Z_g)}\right] + \frac{Z_s\left[1 + j\omega C_{gs}(R_i + Z_g)\right]}{1 + j\omega C_{gs}(R_i + Z_s + Z_g)}. \tag{5}$$

The impedances Z_g and Z_s model the bias and termination loads. Assuming these to be passive, only the voltage-dependent current generator (via the term g_m) contributes to the formation of an active impedance Z_{nr}. The interplay of the elements in Fig. 2 can be determined directly from (5). However, insight into the nature of Z_{nr} is more readily obtained by examining Z_{nr} under a few specific conditions, namely low-frequency excitation and the case of infinite source terminating impedance Z_s.

At very low frequencies, the common-gate circuit provides insufficient loss compensation. This is seen by allowing the frequency to approach zero in (5), resulting in

$$Z_{nr}(f \to 0\text{ Hz}) = R_{ds}(1 + g_m Z_s) + Z_s. \tag{6}$$

Assuming the phase of g_m to be given by $-\omega\tau$ (τ is the FET transit time), then only in the case of highly reactive source impedance loading could $\mathrm{Re}\{Z_{nr}\}$ be negative at low frequencies. The dependence of Z_{nr} on the large drain-to-source resistance R_{ds} indicates that NR circuits load the DA lines minimally at low frequencies.

A second specific condition to examine is when the source termination Z_s becomes infinite. Computer simulations indicate that a large $|Z_s|$ is appropriate for NR compensation across very broad bands. Small values of

$|Z_s|$ tend to decrease the available NR loss compensation because a small, nonresonant source load $|Z_s|$ degrades the voltage division of the input signal across the FET gate-to-source capacitor. The result is a decreased normalized current generator drive ratio $|V_1/V_{nr}|$. When $|Z_s|$ approaches infinity, (5) simplifies to the form

$$Z_{nr} = \frac{R_{ds}}{1 + j\omega C_{ds} R_{ds}} + \frac{1}{j\omega C_{gs}} + R_i + Z_g + \frac{g_m R_{ds}}{j\omega C_{gs}[1 + j\omega C_{ds} R_{ds}]}. \quad (7)$$

The first four terms of (7) are passive in nature, while the fifth term (involving g_m) provides the negative resistance. The real part of the fifth term is

$$\mathrm{Re}\left[\frac{g_m R_{ds}}{j\omega C_{gs}[1 + j\omega C_{ds} R_{ds}]}\right] = -\frac{g_m R_{ds}/(\omega_d C_{gs})}{(1 + j\omega/\omega_d)(1 - j\omega/\omega_d)} \quad (8)$$

where, as before, $\omega_d = 1/(R_{ds} C_{ds})$. For $\omega \geq 2\omega_d$, the negative resistance term of (8) decreases approximately as $1/\omega^2$. Consequently, one can expect an upper frequency to exist at which the net resistance $\mathrm{Re}\{Z_{nr}\}$ becomes positive. Computer simulations of a Honeywell monolithic 0.25×100 μm MODFET equivalent circuit show that the net negative resistance $\mathrm{Re}\{Z_{nr}\}$ extends beyond 70 GHz with various source terminating loads. This FET is discussed later.

Low-gain FET's provide insufficient loss compensation for practical use as common-gate NR circuits. In fact, very low gain FET's cannot overcome the losses attributed to the circuit components R_{ds}, R_i, and Z_g. This is because the NR term of (8) is proportional to g_m. In contrast, as C_{gs} decreases, the NR circuit compensation increases via a larger reflection. This effect may be explained by voltage division concepts: higher impedance gate-to-source capacitances experience greater $|V_1/V_{nr}|$ ratios and thus provide larger current generator drive.

Experimental measurements of the common-gate circuit indicate useful broad-band NR behavior. The de-embedded scattering parameter measurement of S_{11} in Fig. 3 is taken at the drain terminal of a Honeywell common-gate MODFET. Above 18 GHz this 0.25×100 μm MODFET, modeled by the circuit of Fig. 4, presents an impedance for which the real part is negative. The common-gate measurements compare well with FET model simulations, allowing one to implement a NR circuit model during the DA design procedure. (This is to be expected considering (i) the physical implications of the modeling process and (ii) the excellent results obtained by LaRue *et al.* [4] in their extensive FET modeling procedure, for which a single circuit was fitted to common-gate, common-drain, and common-source measurements.)

Computer simulations predict broad bands over which the common-gate circuit provides useful loss compensation. The simulations are based upon internal (monolithic version) MODFET models scaled from the 0.25×100 μm

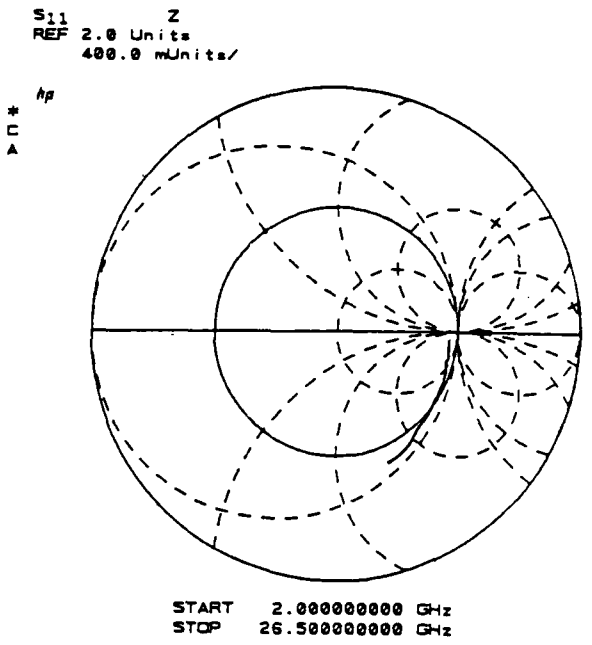

Fig. 3. Drain reflection measurement of a 100×0.25 μm^2 Honeywell MODFET in a common-gate configuration. Above 18 GHz, a negative resistance is displayed.

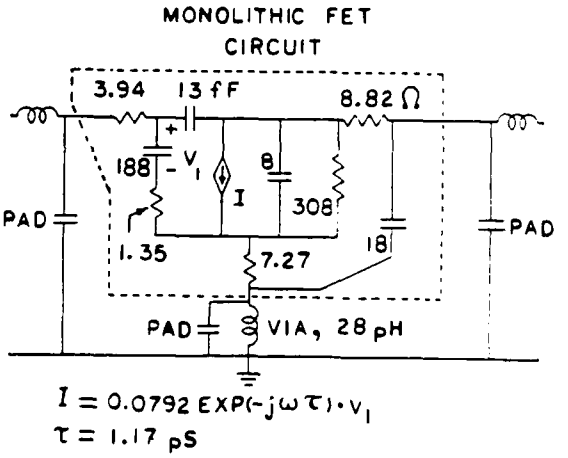

Fig. 4. Equivalent circuit model of the Honeywell 100×0.25 μm^2 MODFET (shown in a common-source configuration). Bonding pad capacitances and wire (and via hole) inductances complicate the basic monolithic circuit model.

MODFET equivalent circuit in Fig. 4. (Fig. 4 includes the hybrid circuit bond pad capacitances and bond wire inductances.) The capacitances, the transconductance, and the conductances scale in proportion to the FET gate width. The simulated scattering parameters of Fig. 5 also describe the common-gate circuit characteristics. By terminating port 2 with a reflective load K_1, one obtains a net input reflection coefficient, K_{in}, at port 1:

$$K_{in} = S_{11} + S_{12} S_{21} K_1 / (1 - S_{22} K_1). \quad (9)$$

The nonzero $S_{12}S_{21}$ term obtained from the parameters of Fig. 5 indicates that source terminations can influence the NR behavior, consistent with (5) and (6). The simulated net input reflection curves of Figs. 6 and 7 demonstrate this. Fig. 6 shows the useful broad-band NR compensation

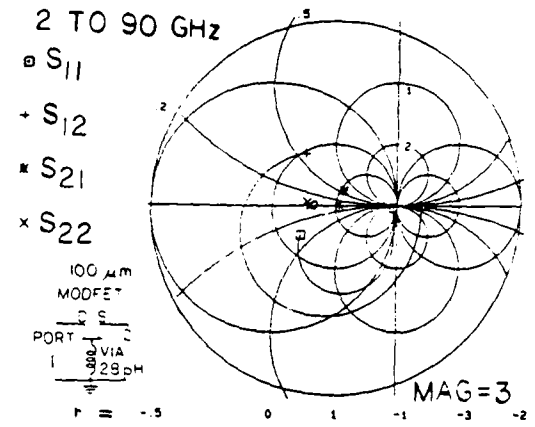

Fig. 5. (TOUCHSTONE) Simulated scattering parameters of the Honeywell (monolithic) MODFET common-gate circuit.

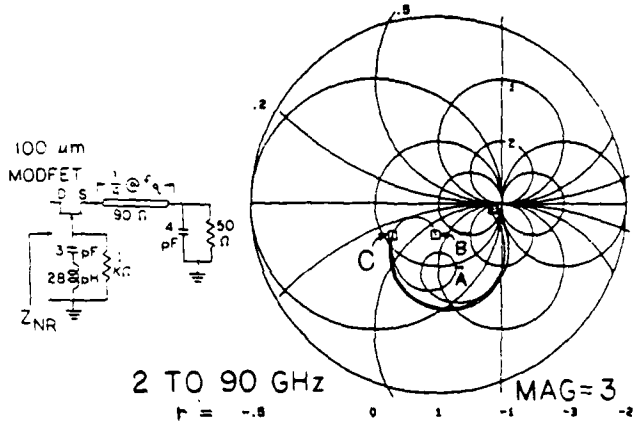

Fig. 7. (TOUCHSTONE) Simulated reflections of the Honeywell common-gate MODFET employing a quarter wave source bias circuit and a gate bias circuit. Curve A: $f_u = 30$ GHz. Curve B: $f_u = 45$ GHz. Curve C: $f_u = 90$ GHz.

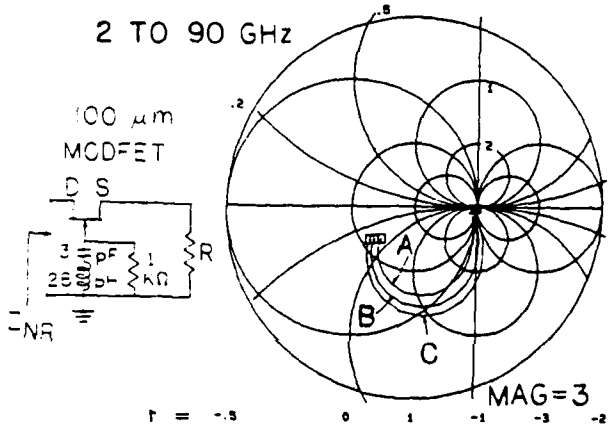

Fig. 6. (TOUCHSTONE) Simulated reflections of the Honeywell common-gate MODFET using resistive source terminations. A gate biasing circuit is included. Curve A: $R = 50\ \Omega$. Curve B: $R = 150\ \Omega$. Curve C: R approaches infinity.

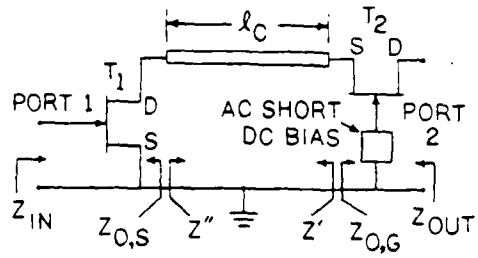

Fig. 8. A cascode circuit, consisting of a common-source FET, a short transmission line, and a common-gate FET.

available using resistive source terminations. In the simulations of Fig. 7 the source termination is formed by a quarter-wavelength (at band center) transmission line terminated by a large capacitance. This allows one to provide FET biases without power losses in bias resistors while maintaining very broad band NR compensation.

V. The Cascode Circuit: Its Use in Distributed Amplifiers

With regard to output line loss compensation, incorporating the common-gate NR circuit with the primary amplifying circuit (a common-source FET) is advantageous in several respects. The source-to-drain signal transmission of the common-gate FET (S_{12} of Fig. 5) is greater than unity magnitude across a large frequency span, whereas the reverse transmission (S_{21} of Fig. 5) remains small. Therefore, connecting the drain of a common-source FET to the source of the common-gate FET can improve the net signal amplification and the reverse isolation. The resulting amplifying circuit, depicted in Fig. 8, is the cascode. The short transmission line, referred to as the cascode line, separates the two transistors, altering the cascode forward gain and the output impedance because of the impedance transformations from $Z_{o,g}$ to Z'' and $Z_{o,s}$ to Z', respectively. High gain cascodes display negative resistance output impedances at moderate to high frequencies because of the common-gate FET output block.

A development of the cascode circuit within the context of loss compensation has been given. However, this circuit is not new to the distributed configuration. Others have reported the use of dual-gate FET's and cascodes in DA applications (cf. [2], [4], [11]), often citing the increased output impedance over that of a common-source FET for increased gain and bandwidth. As trends continue toward higher frequencies and as higher gain FET's are developed, the negative resistance output properties of the cascode must be more closely evaluated in the overall DA design. Since the cascode output, a common-gate FET, is a type of attenuation-compensating network, cascode DA's are included in the DA configuration comparisons in Section VII.

VI. Stability Considerations

For stability, one desires the net input reflection coefficients at the four DA ports to have less than unity magnitude. This translates to four series of conditions, each involving three port terminations and the 16 DA S parameters. Such analyses are very complex and not easily adapted to graphical techniques. In addition, these extensive analyses may be of little practical use with DA's

because of the extreme S parameter variations across the wide bands of operation, especially the phase variations.

A simplified analysis provides insight into the stability conditions. Here the net input reflection at the jth port of the DA, $K_{\text{in},j}$, is approximated by

$$K_{\text{in},j} = S_{jj} + \sum_{\substack{m=1 \\ m \neq j}}^{4} S_{mj} K_{L,m} S_{jm}. \tag{10}$$

The term S_{kl} is a DA four-port scattering parameter and $K_{L,m}$ is the reflection coefficient of the mth port termination. Stable, nonoscillatory behavior is maintained when $|K_{\text{in},j}|$ is less than unity for each of the four ports.

When the phases of the four addends in (10) are equal, the largest reflection magnitude $|K_{\text{in},j}|$ occurs. This constructive addition of reflection terms leads to the four most stringent stability conditions:

$$|K_{\text{in},j}| = |S_{jj}| + \sum_{\substack{m=1 \\ m \neq j}}^{4} |S_{mj} K_{L,m} S_{jm}| \overset{\text{set}}{<} 1, \qquad j = \{1,2,3,4\}. \tag{11}$$

Assuming the four-port scattering parameters to be given, (11) establishes limitations on the set of port termination tolerances $\{|K_{L,m}|\}$ which are based upon the transmission factors $\{|S_{mj} S_{jm}|\}$. The stability criteria have been formulated. The question remains how one specifies port termination tolerances which guarantee stable, insensitive amplifier operation. From the system standpoint, a uniform restriction on port terminations is desirable. This leads to the specification of a maximum termination reflection coefficient, $K_{L,\max}$, for all four ports (of the DA):

$$K_{L,\max} \geq |K_{L,j}|, \qquad j = \{1,2,3,4\}. \tag{12}$$

A tolerance is derived from (11) and (12):

$$K_{L,\max} = \min \left[\left[1 - |S_{jj}|_{\max} \right] \Big/ \left(\sum_{\substack{m=1 \\ m \neq j}}^{4} |S_{mj} S_{jm}| \right) \right] \tag{13}$$

for $j = \{1,2,3,4\}$. When all four ports are terminated by loads with reflection magnitudes less than $K_{L,\max}$, stable, nonoscillatory behavior is maintained. Therefore the term $K_{L,\max}$ is a stability criterion. Equation (13) indicates stability improvement with decreasing $\{|S_{jj}|\}$ and $\{|S_{mj} S_{jm}|\}$. Because the trends of the four-port scattering parameters vary with frequency, it is desirable to calculate a few values of $K_{L,\max}$ based upon midband and upper band edge S parameters.

The transistor characteristics and the DA configuration play dominating roles in determining $K_{L,\max}$. The transistor gains, isolations, and parasitic loading impedances influence the set of transmission factors $\{S_{jm} S_{mj}\}$, which in turn govern $K_{L,\max}$. Similarly, the DA configuration strongly influences the set $\{S_{jm} S_{mj}\}$. Amplifiers employing input line compensation display an increased $|S_{21} S_{12}|$ term. Likewise, DA's with output line compensation (via cascodes) possess an increased $|S_{43} S_{34}|$ value. Not only are the line transmission factors affected by loss compensation, but other pairs of transmission magnitudes may be increased.

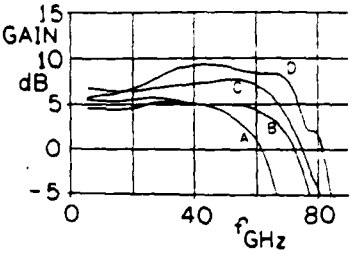

Fig. 9. Frequency response of the four-section DA's. Curve *A*: Conventional configuration. Curve *B*: (Input line) compensated configuration. Curve *C*: Cascode-based configuration. Curve *D*: (Input line) compensated cascode configuration.

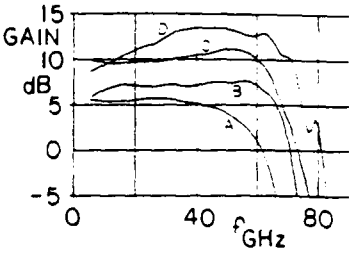

Fig. 10. Response of four DA's. Curve *A*: Conventional configuration (four sections). Curve *B*: (Input line) compensated configuration (eight sections). Curve *C*: (Input line) compensated cascode configuration (eight sections).

Stability Example

A cascode DA with the following midband characteristics is used for stability calculations: S_{41} (dB) = S_{22} (dB) = 10, S_{14} (dB) = S_{23} (dB) < −25, S_{11} (dB) = S_{22} (dB) < −15, S_{44} (dB) = S_{33} (dB) < −15, $|S_{21}| = |S_{12}| = 0.7$, $|S_{41}| = |S_{34}| = 1.2$, S_{31} (dB) = S_{42} (dB) < 7, and S_{13} (dB) = S_{24} (dB) < −30. Using (11)–(13), a value of $K_{L,\max} = 0.487$ is found, which guarantees stable, nonoscillatory operation at midband frequencies.

VII. A Comparison of Circuit Designs

Seven millimeter-wave DA's were simulated and optimized with the aid of the TOUCHSTONE computer program. Each design employs the scaled equivalent circuits of Honeywell 0.25 × 100 μm monolithic MODFET's (Fig. 4). A maximized performance four-section conventional design serves as the basis for comparison. In Fig. 9 the gains of the conventional DA and of three loss compensated DA's employing four sections are given. Three loss compensated DA's employing eight sections are compared to the conventional, four-section DA in Fig. 10. The small sizes of the transistors comprising the seven amplifiers were in part responsible for the very high frequencies achieved. The Appendix contains complete details of the seven amplifier designs.

A. Gains and Bandwidths

Curve *A* of Fig. 9 displays the conventional DA frequency response, a gain of 5.25 dB to 45 GHz. This

TABLE I
PASSBANDS, RETURN LOSSES, AND GAINS OF THE EXAMPLE DISTRIBUTED AMPLIFIERS (FIGS. 9 AND 10)

Amplifier Description	Passband (GHz)	Gain (dB)	Return Losses (dB) Input	Output
Four-section conventional, curves *A*	dc–45	5.25 ± 0.5	> 14.9	14.6
Four-section compensated, curve *B* of Fig. 9	dc–60	4.85 ± 0.5	> 8.5	> 15.2
Four-section cascode, curve *C* of Fig. 9	27–62	7.18 ± 0.5	> 10.3	> 14.4
Four-section compensated, cascode, Curve *D* of Fig. 9	30–62	8.88 ± 0.5	> 7.0	> 15.9
Eight-section compensated, Curve *B* of Fig. 10	10–62	7.15 ± 0.5	> 7.4 > 9, f < 60	> 15.3
Eight-section cascode, curve *C* of Fig. 10	35–60	10.71 ± 0.5	> 13.7	> 13.3
Eight-section compensated cascode, curve *D* of Fig. 10	30–64	12.95 ± 0.5	> 7.2	> 13.9

amplifier has been maximized for gain–bandwidth product (GBWP), achieving a value of 82.4 GHz, and serves as the standard for single-stage response within this transistor family. Because the bandwidth of this amplifier equals the maximum operating frequency, the GBWP equals the gain–maximum operating frequency product (GMFP).

Curve *B* of Fig. 9 is the gain of the DA using input line compensation. The compensation consists of common-gate transistor circuits placed on the input line midway between the amplifying common-source FET's. Here the 4.85 dB gain extends to 60 GHz, resulting in single-stage GBWP and GMFP increases of 27 percent, to 104.9 GHz.

The frequency response of a cascode-based DA is found in curve *C* of Fig. 9. The 7.18 dB gain of this four-section "cascode DA" covers 27 to 62 GHz. This gives a GBWP of 80.0 and a GMFP of 141.7 GHz. The GMFP for this amplifier is 72 percent greater than that of the conventional DA. A high frequency loss was introduced into the output line of the cascode DA to stabilize the onset of the cascode NR output impedance.

Curve *D* of Fig. 9 displays the response of a cascode-based DA which is also compensated on the input line with common-gate NR circuits. This amplifier, termed the compensated cascode DA, does not provide exceptional gain flatness. Nonetheless, the 8.9 dB gain performance between 30 and 65 GHz is considerable. This represents a GBWP of 97.3 GHz and a GMFP of 180.7 GHz, improvements of 18 percent and 119 percent over those of the conventional design. The low frequency slope of curve *D* may be attributed to the onset and gradual increase of NR loss compensation from the common-gate FET's throughout this sample frequency span.

Fig. 10 is a gain comparison of the conventional, four-section DA with three compensated DA's, each using eight sections. Because NR compensation reduces attenuation, an increase in the optimum number of sections results. Hence the full advantage of NR compensation can only be realized if the number of active devices is increased. Curve *A* is the optimized conventional DA (the same DA of Fig. 9, curve *A*). Curve *B* is the frequency response of the DA which uses input line compensation only. The increase from four sections to eight accounts for the gain increase between curve *B* of Fig. 9 and curve *B* of Fig. 10. The MODFET output loss prohibits large gain increases with additional DA sections. Curve *C* of Fig. 10 is the eight-section cascode DA response. Here the usual number of DA sections in a stable design is governed by the input line attenuation. Finally, curve *D* of Fig. 10 shows the response of the eight-section compensated cascode DA. This design shows a low frequency gain slope.

Referring to Fig. 10, the compensated DA has a 7.15 dB gain between 10 and 62 GHz, corresponding to a GBWP of 118.4 GHz and a GMFP of 141.2 GHz. These are 43 percent and 71 percent greater, respectively, than those of the conventional DA design. The eight-section cascode DA has a gain of 10.71 dB across the 35 to 60 GHz span, yielding a GBWP of 85.8 GHz and GMFP of 205.9 GHz, improvements of 4.1 percent and 150 percent over the conventional DA. The eight-section compensated cascode DA gives a GBWP equal to 151.0 GHz and GMFP equal to 284.2 GHz. These are improvements of 83 percent and 245 percent respectively.

The design procedure for the DA's of Figs. 9 and 10 involved gain optimization as well as optimization of return losses and of smooth, controlled transmissions across the DA input and output lines (S_{21} and S_{43}). These are important for stability, power performance and modular system applications. Table I provides a summary of simu-

TABLE II
COMPARISON OF MAXIMUM DA OUTPUT POWERS: PROJECTED MAXIMUM OUTPUT POWERS OF THE CONVENTIONAL DA (CURVE *A* OF FIG. 10), THE CASCODE DA (CURVE *C*), AND THE COMPENSATED CASCODE DA (CURVE *D*) ARE COMPARED TO THAT OF THE INPUT LINE COMPENSATED DA (CURVE *B*)

f (GHz)	P_{max} (Curve *B* of Fig. 10) / P_{max} (Curve *A* of Fig. 10)	P_{max} (Curve *B* of Fig. 10) / P_{max} (Curve *C* of Fig. 10)	P_{max} (Curve *B* of Fig. 10) / P_{max} (Curve *D* of Fig. 10)
25	4.2	0.77	1.0
35	2.4	0.77	1.0
45	2.6	1.1	1.2
55	out of passband	1.9	1.8

lated return losses and responses of the seven amplifiers.

B. Power Considerations

The increased gains of the six NR loss-compensated DA's of curves *B*, *C*, and *D* in Figs. 9 and 10 do not necessarily lead to increased maximum output power levels. Power saturation mechanisms, especially those of cascodes and dual gate FET's, can adversely affect the allowed maximum DA input power and thereby lessen the maximum output power. Each FET has limited voltage swings across its nodes for linear performance. The circuit configuration, the component values, the input power level, and the specific location within the circuit influence the FET ac voltages. In the cascode DA, the FET ac voltages are especially sensitive to the cascode line length(s). The ac voltage constraints of the second (common-gate) cascode FET often restrict the voltage swing across the first cascode FET to less than its inherent dynamic range. Hence, input power may have to be reduced. This might explain why cascode and dual-gate DA's reported in the literature have not greatly extended output power levels despite showing improved gain–bandwidth products over conventional DA's.

A study of projected maximum output powers shows the input line compensated DA (curve *B*, Fig. 10) to surpass both the cascode DA and the compensated cascode DA (curves *C* and *D*, Fig. 10) in performance by as much as 90 percent at high frequencies (55 GHz). Power performance is summarized in Table II. The primary saturation mechanism was assumed to be the ac gate-to-source voltage swing. It must be stressed that all DA design examples in this paper were optimized for GBWP, not for maximum output power.

It appears that crucial signal saturation mechanisms must be closely examined throughout the design process to ensure maximized power output, regardless of the DA configuration. Preliminary studies do indicate that the appropriate NR loss compensated DA designs can drastically improve the maximum DA output power levels.

VIII. CONCLUSIONS

Enhanced DA frequency responses are possible by lessening or eliminating the signal losses present along the input and/or the output lines. The new loss compensation technique presented here involves a "negative resistance" circuit placed in shunt on the lossy line. That circuit, based upon a common-gate FET, has an impedance characterized by negative resistance and a capacitive reactance. Two design simulations using the NR circuit for input line loss compensation have shown GBWP and GMFP increases of 27 percent and 71 percent over those of the conventional DA design. Cascodes, amplifiers related to the negative resistance circuit, were discussed. Simulations of two cascode DA design examples predict GMFP increases of 72 percent and 150 percent beyond that of the conventional DA. Two DA simulations of loss compensation on both DA lines (via the compensated cascode DA) have shown GMFP increases of 119 percent and 245 percent. Lastly, a first-order, four-port stability analysis has been presented, yielding insight into DA loading and stability.

The use of NR loss compensation on either of the DA lines allows substantially higher single-stage gain–bandwidth product performance than the maximum product possible with conventional DA designs. The impact of this performance enhancement is twofold: improvements in the single-stage gain often promise increased maximum output power, while increases in bandwidth are desirable for modular system design.

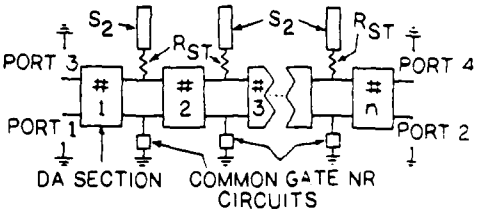

Fig. 11. The general configuration of the seven distributed amplifier (DA) design examples.

APPENDIX
DISTRIBUTED AMPLIFIER (DA) DESIGN DETAILS

The details of the seven DA designs are found in Figs. 11–14 and Tables III and IV. Fig. 11 is a generalized block diagram of the seven DA's. A typical gain section detail (DA section = k) may be found in Fig. 12. Two amplifying circuits, the common-source transistor of Fig. 13(a) and the cascode circuit of Fig. 13(b), have been used in the designs. In Fig. 14 is the common-gate negative resistance circuit. Tables III and IV list appropriate values for the circuit elements. The microstrip lines (TL_n) and open-ended stubs (S_1, S_2) have widths and lengths given in μm and denoted by 'w' and 'l', respectively. A (GaAs) substrate of

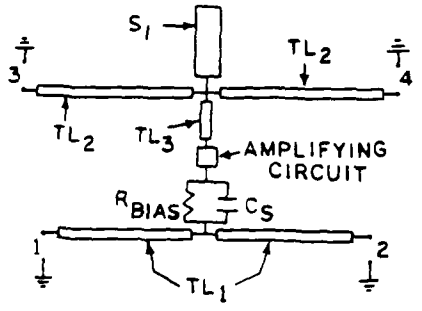

Fig. 12. Distributed amplifier gain section detail.

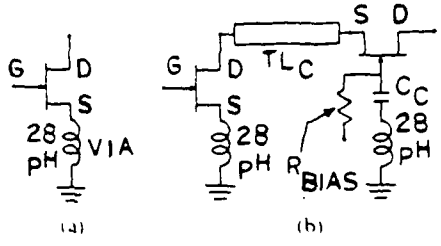

Fig. 13. Schematics of the amplifying circuits used in this study. (a) A common-source FET. (b) A cascode circuit.

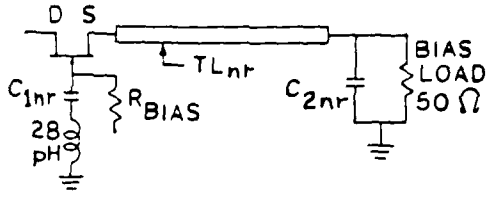

Fig. 14. The common-gate negative resistance circuit.

TABLE III
ELEMENT VALUES FOR THE FOUR-SECTION DA'S

	conventional	(input line) compensated	cascode	compenstd. cascode
TL_1	w = 12.7	w = 12.7	w = 12.7	w = 12.7
(microns)	l = 128.2	l = 98.6	l = 99.6	l = 98.3
TL_2	w = 12.7	w = 12.7	w = 12.7	w = 19.8
(microns)	l = 160.8	l = 155.0	l = 128.1	l = 149.6
TL_3	w = 12.7	w = 12.7	(absent)	(absent)
(microns)	l = 120.0	l = 65.0		
S_1	(absent)	w = 19.8	(absent)	w = 35.0
(microns)		l = 18.5		l = 14.9
S_2	(absent)	w = 19.8	w = 35.0	w = 19.8
(microns)		l = 27.8	l = 62.2	l = 90.7
R_{st}	(absent)	0 ohms, no loss	302	76
(ohms)				
R_{bias}	1000	1000	1000	1000
(ohms)				
C_s	0.305	0.348	0.366	0.369
(pF)				
Common source FET amplifying circuit	60 micron FETs	60 micron FETs	(not utilized)	(not utilized)
Cascode amplifying circuit	(not utilized)	(not utilized)	60 micron FETs C_c = 3.0 TL_c: w = 12.7 l = 87.6	60 micron FETs C_c = 3.0 TL_c: w = 12.7 l = 340.0
Negative resistance compensat'n circuit -- input line	(not utilized)	90 micron FETs C_{1nr} = 2.5 C_{2nr} = 4.0 TL_{nr}: w = 12.7 l = 605.6	(not utilized)	90 micron FETs C_{1nr} = 3.0 C_{2nr} = 3.5 TL_{nr}: w = 12.7 l = 525.9

TABLE IV
ELEMENT VALUES FOR THE EIGHT-SECTION DA'S

	(input line) compensated	cascode	compensated cascode
TL_1	w = 12.7	w = 12.7	w = 12.7
(microns)	l = 103.1	l = 95.0	l = 101.3
TL_2	w = 12.7	w = 12.7	w = 19.8
(microns)	l = 154.9	l = 99.5	l = 147.7
TL_3	w = 12.7	w = 12.7	w = 12.7
(microns)	l = 19.6	l = 17.5	l = 4.3
S_1	w = 19.8	(absent)	w = 35.0
(microns)	l = 55.7		l = 26.9
S_2	w = 19.8	w = 35.0	w = 19.8
(microns)	l = 83.6	l = 94.7	l = 123.0
R_{st}	0	226	50
(ohms)	(no loss)		
R_{bias}	1000	1000	1000
(ohms)			
C_s	0.154	0.139	0.176
(pF)			
Common source FET amplifying circuit	60 micron FETs	(not utilized)	(not utilized)
Cascode amplifying circuit	(not utilized)	60 micron FETs C_c = 3.0 TL_c: w = 12.7 l = 118.9	60 micron FETs C_c = 3.0 TL_c: w = 12.7 l = 330.0
Negative resistance compensation circuit -- input line	90 micron FETs C_{1nr} = 2.5 C_{2nr} = 4.0 TL_{nr}: w = 12.7 l = 579.9	(not utilized)	90 micron FETs C_{1nr} = 3.0 C_{2nr} = 3.5 TL_{nr}: w = 12.7 l = 525.9

thickness 0.004 in and relative permittivity 12.9 was used in the simulations.

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Optimizing the Power-Added Efficiency of a Class B GaAs FET Amplifier

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Abstract

The paper reports on a design routine which optimizes the power-added efficiency of a Class B microwave amplifier stage. Experimental results at 4.4 GHz are reported which support the procedure and show efficiency increases of 15% when low impedance loading at even harmonic frequencies are provided.

Introduction

There are a number of variables which must be considered when designing a GaAs FET amplifier for maximum power-added efficiency. These variables include: conduction angle, drain bias voltage and the load impedance at both the fundamental and harmonic frequencies. Conduction angle is a variable because of the non-abrupt pinch-off associated with GaAs FETs. Predicting and experimentally determining optimum values for these variables is addressed in this paper in which the design and testing of a 4.4 GHz amplifier is reported.

One possible approach to the problem of maximizing power-added efficiency involves idealizing the device characteristics and circuit to the point where a simple analysis is possible. A much more accurate and time-consuming approach would be to use a large-signal simulation program such as SPICE or a more time efficient method such as the harmonic balance simulation technique. An optimization routine which uses a simulation program to test various combinations of the aforementioned variables can then be used to predict the optimum power-added efficiency for a particular device.

The method presented in this paper falls between the above approaches in complexity yet yields insight and fairly accurate solutions. The measured data required consists of device I-V data and one large-signal gain measurement at the microwave frequency of interest. The method is based on a simple circuit model from which the power-added efficiencies, resulting from a specific combination of the variables, can be calculated.

Similar to the harmonic balance method this simulation iterates between time domain and frequency domain solutions until agreement is reached.

RF I-V Measurement

RF (>1MHz) I-V measurements are more accurate and relevant to microwave behavior than DC I-V measurements for three reasons: 1. Trapping effects are included.[1] 2. The instantaneous channel temperature can be held controlled while the measurement is being made. 3. The device dissipation at RF can be made to match the device dissipation at the microwave frequency.

While the device was operating at 11MHz, the instantaneous gate and drain voltages and drain current were measured with probes and an oscilloscope. A schematic of the measurement set-up is shown in Fig. 1.

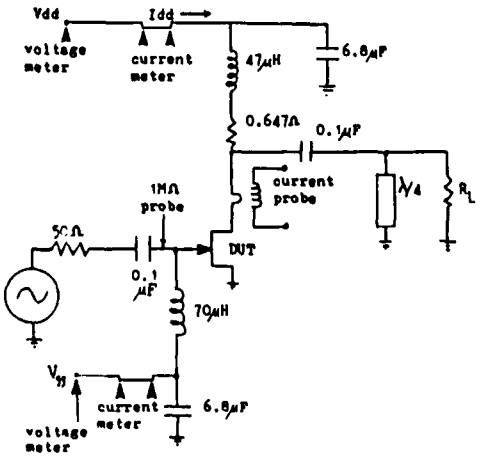

Fig. 1. RF I-V curve tracer.

The data points were gathered at 1V increments of V_{GS} and the associated V_{DS} and I_{DS} were

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recorded. Next the drain voltage bias was increased by 1V and another set of data points were measured in the same way. The load resistance was adjusted as V_{DD} was increased to keep the power dissipated in the device constant. With this technique, device dissipation at 11MHz could be adjusted to match device dissipation at the microwave frequency of interest. Therefore the channel temperature was made to equal the channel temperature at the microwave operation being modelled. The rate of 11MHz insured that trapping and thermal time constants were not affecting the measurement.

An example of the measured current waveforms for increasingly larger V_{DD} are shown in Fig. 2.

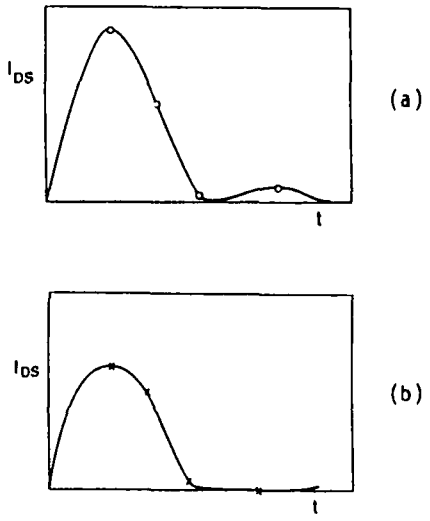

Fig. 2. Typical measured drain currents.

In waveform 2(a), the peak of the current is occurring below the knee of the I-V curves thus distorting the waveform. In waveform 2(b) drain-to-gate breakdown current is evident. Figure 3 shows how the data points result in the family of RF output characteristics.

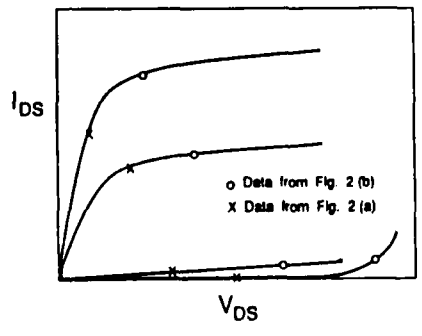

Fig. 3. RF output characteristics generated from data of Fig. 2.

Optimization/Simulation Program

Figure 4 shows the circuit model used for the simulation routine. The model includes the effects of the gate and drain bias voltages. The drain to source capacitance, C_{DS}, which has been separated from the "intrinsic FET." A complex load is assumed but the load inductance is adjusted to cancel the reactance of C_{DS} at high efficiency operation. Therefore the "intrinsic FET" drives a purely resistive load in the model.

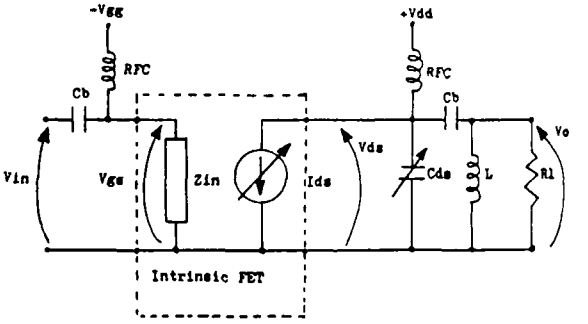

Fig. 4. Circuit model used in optimization program

The program computes the highest power-added efficiency possible for conduction angles between class A and B. The optimum drain bias voltage and load resistance for each conduction angle is also predicted.

The program works as follows. For a given conduction angle, a sinusoidal gate voltage waveform is calculated on the basis of the pinch-off voltage of that device. With a selection of drain bias voltage, V_{DD}, and load resistance, R_L, together with an initial drain to source voltage amplitude, V_{DS}, a corresponding drain current waveform can be computed from the I-V data. Rather than fitting the I-V data to an equation, a look-up table of the measured I-V data and an interpolation routine gives I_{DS} as a function of V_{GS} and V_{DS}. A discrete Fourier transform is performed on the drain current waveform to calculate the fundamental component. The DC component of the current is also calculated. The fundamental component of the current is multiplied by the load resistance to calculate the magnitude of the new and more accurate time domain solution of V_{DS}. This loop continues until a solution ceases to change appreciably.

Because V_{DD} was selected and the DC drain current was computed, the input DC power is known. The AC drain voltage and current were found and assumed to be in phase so the output power can also be determined. Thus drain efficiency can be computed. The amount of power delivered to the gate is computed on the basis of the magnitude of the driving voltage. This input

power is correlated to the microwave gain data taken under known operating conditions. With the input and output microwave power calculated along with the DC power, the power-added efficiency is determined.

A search routine tests various combinations of V_{DD} and R_L until the optimum combination is found which maximizes the power-added efficiency. Next another conduction angle is chosen and the above process repeats itself.

Evaluation of Power and Efficiency Measurements

The "intrinsic FET" model, shown in Figure 4 uses an ideal representation of the matching circuit on the output of the FET. The actual loading circuit used in the experiment, shown in Figure 6, utilizes a short-circuited quarter-wave stub to obtain harmonic cancellation, followed by a matching circuit that provides optimum efficiency at the fundamental frequency. Intuitively it is straightforward to see that reducing the harmonic output power improves the efficiency of an amplifier. Specifically, suppressing harmonic voltage while retaining a half sine wave pulsating current minimizes device dissipation. To see this effect first consider the case where the fundamental signal and the 2nd harmonic are terminated in a 50Ω load.

The well-known upper limit Class "B" for collector efficiency, η, for this case is 78.5% ($\pi/4$). The efficiency is given by

$$\eta = \frac{P_{DC}-P_{DISS}}{P_{DC}} \% \ , \qquad (1)$$

where we assume $V_{sat} = 0$ and a sharp cutoff in the characteristics of the FET, see Fig. 5. Now we can write,

$$\frac{V_1}{I_1} = \frac{V_2}{I_2} \qquad (2)$$

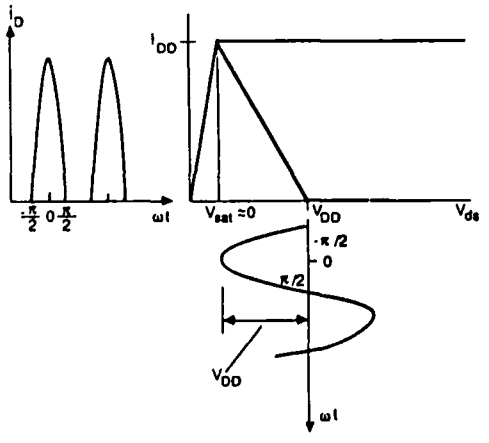

Fig. 5. Ideal RF output characteristics

To determine V_2 equate the peak value of the halfwave sinusoid to the saturation current, I_{DD}, and V_1 to V_{DD}, see Fig. 5. Then using the Fourier coefficients of a halfwave sinusoid,

$$I_{DC} = \frac{I_{DD}}{\pi} \ , \quad I_1 = \frac{I_{DD}}{2} \ , \quad I_2 = \frac{2I_{DD}}{3\pi} \qquad (3)$$

We can write V_2 as:

$$V_2 = \frac{4V_{DD}}{3\pi} \qquad (4)$$

So the power dissipated in the device due to the presence of the second harmonic voltage is

$$P_{2DISS} = \frac{1}{2\pi}\int_{-\pi/2}^{\pi/2} (I_{DD}\cos\omega t)\left(\frac{4V_{DD}}{3\pi}\sin 2\omega t\right)d\omega t = \frac{4V_{DD}I_{DD}}{9\pi^2} \qquad (5)$$

This term, substituted into P_{DISS} in Eq. 1, reduces the collector efficiency by 14.1%. A reduction in the harmonic load reduces the harmonic voltage while the current waveform retains its nonlinearity. In the experiment performed we reduced the harmonic load from 50Ω to 5Ω, ideally this represents an increase in efficiency from 64.4% to 77.1%, a 13.3% change in collector efficiency.

The power gain and efficiency measurements were obtained with the set-up shown in Fig. 6.

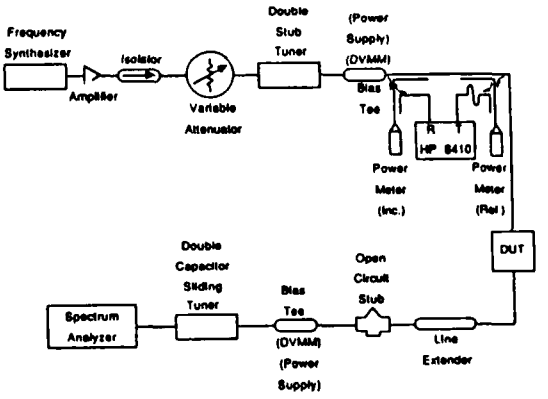

Fig. 6. Microwave efficiency experiment.

This set-up provides the means for measuring input power, input reflection coefficient and the output power. With these measurements, along with the bias levels, we can determine the power gain, conduction angle and the power-added efficiency. The harmonic loading consists of a coaxial line extender and a tee (type SMA). Due to obvious DC biasing problems in using a shorted quarter-wave stub, an open SMA barrel was connected to the tee

and the nonideal nature of the tee provided a frequency response that resembles a shorted quarter-wave stub. This quarter-wave stub provides a second harmonic load of 5Ω, and the fundamental load is completely determined by the double stub tuner. The effective short at the harmonic frequencies provides a direct path for the harmonic currents to the source, while also suppressing the harmonic voltages induced by the transistor.

Results and Conclusions

The results of the simulation and measurements are shown in Figs. 7, 8 and Table 1. The plots show the amount of agreement between the simulated versus measured results.

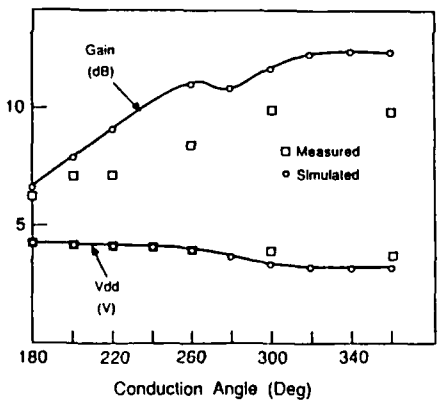

Fig. 7. Gain and V_{DD} versus conduction angle.

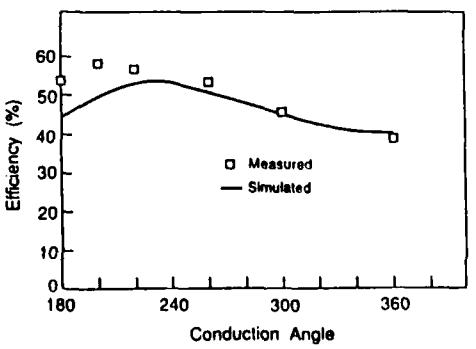

Fig. 8. Power-added efficiency versus conduction angle.

Note in Figure 8 the power-added efficiency peaks at a conduction angle of 200°, due to the non-abrupt pinch-off characteristics of the GaAs FETs. In Table 1, the effect of the second harmonic impedance is shown to and agrees with expected changes in efficiency computed above.

Table 1

Fundamental Load (ohms)	Harmonic Load (ohms)	Power-added Efficiency	Change in Efficiency
42-j20.0	38-j3	46.3%	-
42-j21.5	5.0	61.7%	15.4%
25.0	42+j12.5	31.2%	-
25.0	5.0	45.6%	14.4%

Note: Bias levels were held constant for both harmonic load cases.

The authors would like to add that a monolithic version of the experiment is being processed and is expected to show clearly the effect of harmonic loading on power-added efficiency. This technique, after refinement for better accuracy, holds promise for: 1) evaluating new microwave power devices, 2) gaining insight into the inter-relations of MESFET characteristics which determine efficiency, and 3) aiding in initial designs of power amplifiers.

Acknowledgements

We would like to thank Steve Nelson of Texas Instruments for providing the transistor test fixture and the 1200 μm power GaAsFET chip for the experiment.

Reference

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A LARGE SIGNAL NONLINEAR MODFET MODEL FROM SMALL SIGNAL S-PARAMETERS*

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ABSTRACT

A general technique for predicting the FET large signal performance has been developed. The technique is based entirely on experimental data (small signal S-parameters at different bias points) and therefore is independent of the structure of the FET. Large signal measurements confirm the validity of the model.

I. INTRODUCTION

Modulation doped FETs (MODFETS) have already been proven to have good noise performance for microwave applications (1). MODFETs are also well suited for class B amplifiers, since their transfer characteristic can be approximated by a piecewise linear curve and this leads to a large signal transconductance independent of the signal level. However, there are few large signal models available and the determination of the parameters of such models is difficult or requires special equipment. Furthermore, the models cannot be used conveniently in common CAD programs.

The model and measurement techniques presented here overcome these problems. Software requirements include: a program (like TOUCHSTONE™) to fit an equivalent circuit to S parameter data; a simple least square polynomial approximation program; and the popular SPICE for nonlinear time domain simulations. Hardware requirements are basically limited to a network analyzer to carry out the small signal S parameter measurements.

II. NONLINEAR MODFET CIRCUIT MODEL

A. Circuit Elements

The nonlinear circuit proposed is an extension of a widely used small signal equivalent circuit in which the nonlinearity of $C_{gs}(v_1)$ and $Ids(v_1,v_{ds})$ is taken into account (see Fig. 1). In this circuit $Ids(v_1,v_{ds})$ models the nonlinearities of the transconductance (g_m) and the output conductance (G_0) through Eqs. 1 and 2:

$$G_0(v_1,v_{ds}) = \frac{\partial I_{ds}(v_1,v_{ds})}{\partial v_{ds}} \qquad (1)$$

$$g_m(v_1,v_{ds}) = \frac{\partial I_{ds}(v_1,v_{ds})}{\partial v_1} \qquad (2)$$

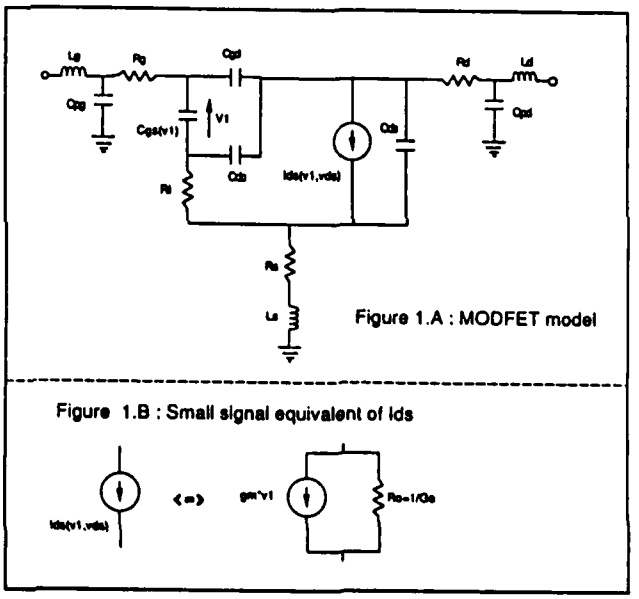


Figure 1.A : MODFET model

Figure 1.B : Small signal equivalent of Ids

B. Determination of the Linear Element Values

The values of C_{ds} and the extrinsic elements have been determined for a 300μm SONY MODFET by measuring its S parameters at V_{DS},V_{GS} = 0 and fitting its equivalent circuit at this bias point (Fig. 2) (2), (3) (See Table 1). In our model, only C_{gs} and I_{ds} are allowed to be voltage-dependent. To describe this dependence we have to adjust g_m, G_0, C_{gs}, R_i, C_{gd} and C_{dc} in Fig. 1 to match the S parameters at several bias points. Only the first three parameters are used to characterize the nonlinear behavior of $C_{gs}(v_1)$ and $I_{ds}(v_1,v_{ds})$(4). The linearized equivalents of R_i, C_{gd}, and C_{dc} are found by averaging their values at these bias points. The obtained values are:

*This work is supported by Honeywell Inc., ONR and Caja de Pensiones (Barcelona, Spain).

R_i = 1.22 Ω; C_{gd} = 0.0438 pF; C_{dc} = 0.0518 pF

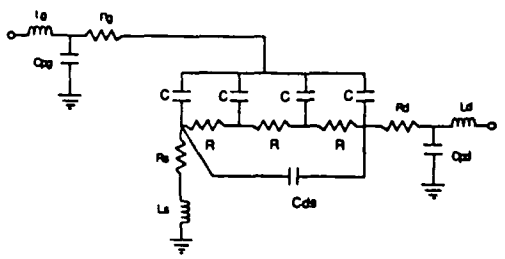


Figure 2 Zero-bias equivalent circuit

Table 1: Linear elements from zero bias circuit

L_d = 0.0741 nH	L_g = 0.0478 nH	L_s = 0.0588 nH
R_d = 1.39 Ω	R_g = 1.36 Ω	R_s = 1.22 Ω
C_{ds} = 0.0219 pF	C_{pg} = 0.0267 pF	C_{pd} = 0.0371 pF

C. Determination of $Ids(v_1,v_{ds})$

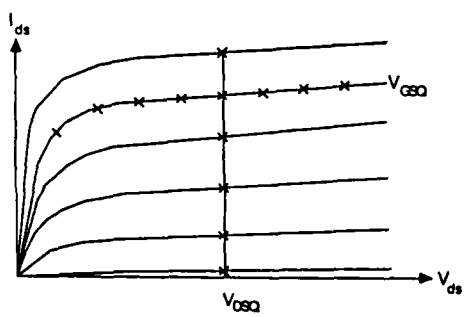


Figure 3 Distribution of the bias points

Figure 3 shows the distribution of the bias points for which a small signal equivalent circuit has been determined. If we assume that $Ids(v_1,v_{ds})$ can be expressed as a product of two one-variable functions; i.e.:

$$I_{ds}(v_1,v_{ds}) = p_g(v_1)p_d(v_{ds}) \qquad (3)$$

$p_g(v_1)$ can be found from the transfer function at $v_{ds} = V_{DSQ}$:

$$p_g(v_1) = \frac{I_{ds}(v_1,V_{DSQ})}{p_d(V_{DSQ})} \qquad (4)$$

At this point we can set $pd(V_{DSQ}) = 1$; then $p_g(v_1)$ is forced to take the values of the transfer characteristic. From Eq. 2 and knowing that

$$I_{ds}(V_T,V_{DSQ}) = 0 \qquad (5)$$

(V_T being the pinch-off voltage), we can write

$$p_g(v_1) = \int_{V_T}^{v_1} g_m(u,V_{DSQ})du \qquad (6)$$

which allows us to evaluate the v_1 dependence of I_{ds} from the measured g_m at several bias points. Figure 4 shows the values of g_m measured for V_{GS} ranging from -1.4V to 0.4V and $V_{DS} = V_{DSQ} = 2V$ and their corresponding values of p_g (or $Ids(v_1,V_{DSQ})$) found with Eq. 6.

Similar steps are taken to determine the dependence of I_{ds} with v_{ds}: from Eqs. 1 and 3 we know that

$$G_0(V_{GSQ},v_{ds}) = p_g(V_{GSQ})p_d'(v_{ds}) \qquad (7)$$

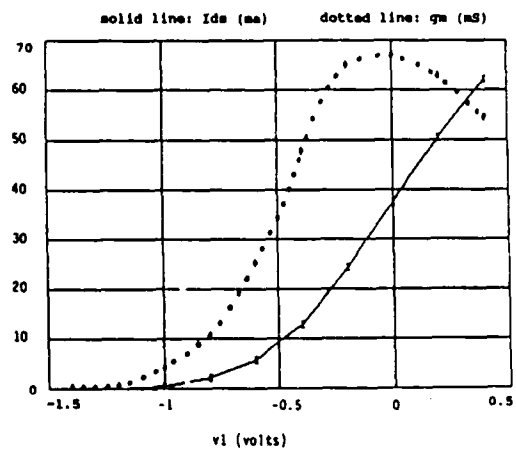


FIGURE 4: TRANSCONDUCTANCE AND TRANSFER CURVE FOR Vds=VDSQ=2V

but $p_g(V_{GSQ}) = I_{ds}(V_{GSQ},V_{DSQ})$ so

$$p_d'(v_{ds}) = \frac{G_0(V_{GSQ},v_{ds})}{I_{ds}(V_{GSQ},V_{DSQ})} \qquad (8)$$

This equation, with the condition $p_d(V_{DSQ}) = 1$ leads to p_d for the nonzero values of v_{ds}:

$$p_d(v_{ds}) = 1 + \frac{1}{I_{ds}(V_{GSQ},V_{DSQ})} \int_{V_{DSQ}}^{v_{ds}} G_0(V_{GSQ},u)du \qquad (9)$$

Also, since $I_{ds}(v_1,0) = 0$, p_d has to be zero for $v_{ds} = 0$.

In Table 2, the practical application of Eq. 9 is shown: Starting from the values of $G_0(V_{GSQ},V_{DS})$ and performing the numerical integration indicated in Eq. 9, the values of $p_d(V_{DS})$ are found for V_{DS} ranging from 0.5 to 4V.

D. Polynomial fitting of $p_g(v_1)$, $p_d(v_{ds})$ and $C_{gs}(v_1)$ for class B applications

The approach discussed so far has allowed us to describe the voltage dependencies with one-variable functions. What is needed now is to express these functions in a form that can be

Table 2 - Determination of $P_d(V_{DS})$ from Output Conductance Data ($V_{GS} = V_{GSQ} = -0.2V$)

V_{DS}	0.5	1.0	2.0	3.0	4.0
G_0 (mS)	18.9751	8.2583	5.2548	3.7447	3.4330
$\int_{V_{DSQ}}^{V_{DS}} G_0(mA)$	-13.5647	-6.7563	0	4.4995	8.0884
$P_d(V_{DS})$	0.4408	0.7215	1	1.1855	1.3334

handled by a CAD program. Our work has been focused towards getting a model for SPICE, whose user-defined nonlinearities have to be expressed in polynomial form.

There are several methods to fit a polynomial to a set of data. Our choice is the one described by Hayes (5) in which the sum of the squares of the residual error is minimized by using a sum of orthogonal polynomials. Other algorithms as well as commericial software can be used for this purpose.

For simulating class A operation we need to get data at $V_T < v_1 < v_{max}$ and carry out the fitting of $p_g(v_1)$ and $C_{gs}(v_1)$ in this range. However, for class B and C operation it might not be necessary to take measurements in the whole range of values of v_1. This is because we know beforehand that $p_g(0) = 0$ for $v_1 < V_T$ and that $C_{gs}(v_1)$ behaves smoothly in this range. Advantage is taken of both facts to limit the measurement range to $V_T < v_1 < v_{1max}$. In our case we are interested in class B operation and our device has $V_T = -1V$ and $v_{1max} = 0.4V$ which makes our class B range $-2.4 \leq v_1 \leq 0.4$.

Extrapolation of p_g below the pinch-off voltage consists of adding zeros at discrete values of v_1. Figure 5 shows the process for our particular case (5.4μA rms error with a 10 degree polynomial).

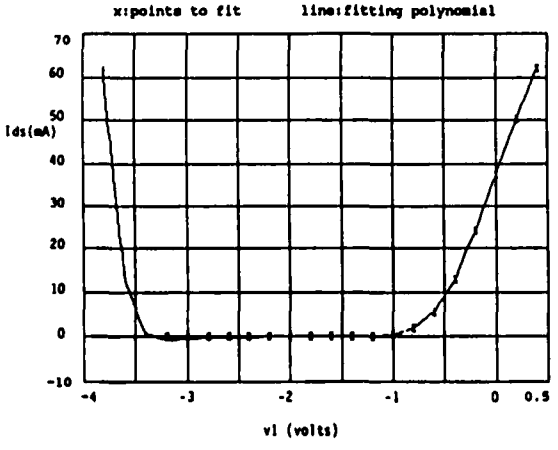


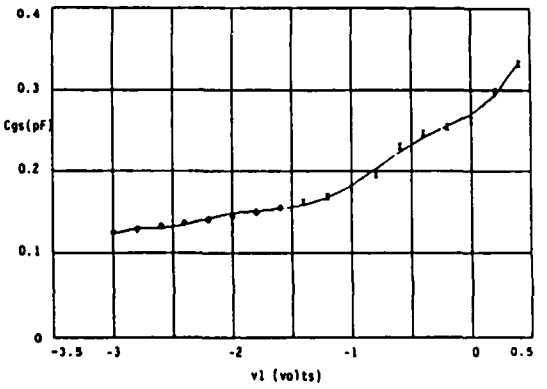
FIGURE 5: POLYNOMIAL FITTING OF THE TRANSFER CURVE

Note that for the lower values of v_1, $p_g(v_1)$ is quite different from zero. This is a typical characteristic of polynomial fitting, i.e. the (absolute) error tends to be higher at the extremes of the fitting interval. Therefore, we can expect to have the highest relative errors at the leftmost extreme of the transfer characteristic where the currents are small but the fitting error can be high. To avoid this effect, a few zeros were added at values of v_1 less than -2.4V.

Extrapolation of $C_{gs}(v_1)$ is more involved. First, a coefficient m has to be found to fit the measured values of C_{gs} to the expression

$$C_{gs}(v_1) = \frac{C_{gs}(0)}{(1 - \frac{v_1}{0.8})^m} \qquad (10)$$

which can be later used to find C_{gs} for $v_1 < V_T$. Figure 6 summarizes this process for our particular case ($m = 0.474$). A 3.8 fF rms error is obtained with an 8 degree polynomial.



x : measured values o: extrapolated values
line: fitting polynomial

FIGURE 6: POLYNOMIAL FITTING OF Cgs(vl) AT Vds=VDSQ=2V

Finally, $p_d(v_{ds})$ has to be interpolated to the values shown in Table 2 and the point $P_d(0) = 0$. Note that since interpolation is a particular case of polynomial fitting, the same software that has been used to fit $p_g(v_1)$ and $C_{gs}(v_1)$ can now be used to interpolate $p_d(v_{ds})$.

III. EXPERIMENTAL RESULTS

Measurements at 10 GHz on a SONY MODFET 2SK677H5 were made to confirm the three basic nonlinear effects:

- Nonlinearity in C_{gs}
- Nonlinear dependence of Ids with v_{ds}
- Nonlinear dependence of Ids with v_1

The accuracy of the nonlinear behavior of $C_{gs}(v_1)$ was checked by measuring the large signal S_{11} and comparing it with simulated data. This is shown in Figure 7, where the measured class A and class B S_{11} are compared to the calculated ones for two values of incident power.

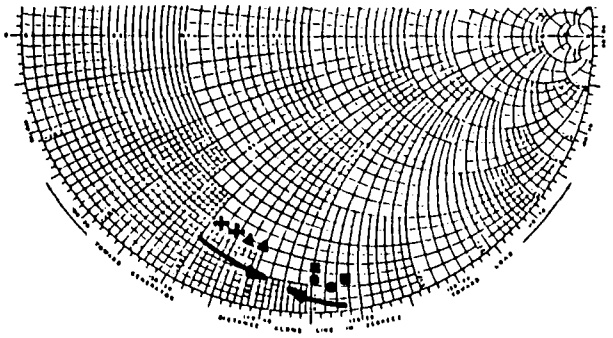


FIGURE 7: LARGE SIGNAL S11

+ Measured Class A } V_{DS} = 3V V_{GS} = -0.31V
▲ Simulated Class A } $P_{IN\ min}$ = -5.86 dBm $P_{IN\ max}$ = 6.64 dBm

● Measured Class B } V_{DS} = 3V V_{GS} = -1V
■ Simulated Class B } $P_{IN\ min}$ = -5.86 dBm $P_{IN\ max}$ = 9.14 dBm

-The arrows indicate the change in S11 with increasing P_{IN}

Similarly, the large signal S_{22} is expected to be sensitive to the nonlinear dependence of I_{ds} with v_{ds}. Figure 8 shows comparitive results of this parameter at two bias levels. (This parameter showed low sensitivity to the incident power).

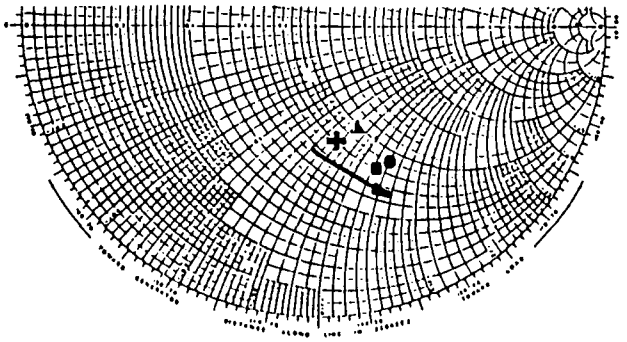


FIGURE 8: LARGE SIGNAL S22

+ Measured } V_{DS} = 1V ; V_{GS} = -0.31V
▲ Simulated }

● Measured } V_{DS} = 3V ; V_{GS} = -0.31V
■ Simulated }

-Incident Power: P_{IN} = 4.14dBm

-The arrow indicates the change in S22 with increasing V_{DS}

Finally, the accuracy in the modeled transfer characteristic was checked by comparing the measured DC current generated in class B operation to the calculated value. This is shown in Figure 9 and again, good agreement is found.

IV. CONCLUSIONS

FET modeling can be done with little hardware and common software. The proposed model does not make any assumption as to the physical structure of the FET, and the CAD simulations are in good agreement with large signal measurements.

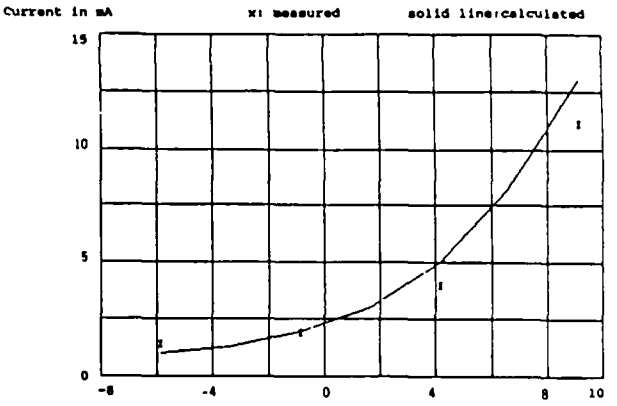


FIGURE 9: DC CURRENT GENERATED IN CLASS B OPERATION

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BAND-PASS DISTRIBUTED AMPLIFIERS

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KEY TERMS

Distributed amplifiers, travelling-wave amplifiers, wideband amplifiers, band-pass amplifiers, mm-wave amplifiers

ABSTRACT

A novel band-pass distributed amplifier design concept is presented. The amplifier can be realized in monolithic form using GaAs FETs. The amplifier has excellent wideband gain and phase response characteristics. It shows promise for applications in the millimeter wave region. In this paper the results of analytical modelling as well as computer simulations are discussed.

I. INTRODUCTION

The wide bandwidth and output power capabilities of GaAs FET MMIC distributed amplifiers are well known [1, 2]. In conventional distributed amplifiers the FET gate and drain capacitances together with external inductors (electrically short, high impedance microstriplines) form artificial transmission lines. The input and output transmission lines, known as gate and drain lines, respectively, are essentially low-pass structures. The 1-dB bandwidth of these amplifiers is limited and can at best approach the cutoff frequency of the lines as shown in [1].

In this paper a novel band-pass distributed amplifier design concept is presented. This approach enables one to design distributed amplifiers having wideband gain response beyond the cutoff frequencies of conventional low-pass distributed amplifiers. Band-pass distributed amplifiers utilizing vacuum tubes have been investigated [3, 4]. These amplifiers were designed and built in the RF frequency range using lumped circuit elements. Therefore the designers had to contend with large physical sizes of the components. With the advent of GaAs monolithic integrated circuit technology and the availability of GaAs FETs that operate in the millimeter-wave region, the band-pass distributed amplifier has attracted attention again.

A hybrid integrated circuit band-pass distributed amplifier using GaAs FETs and operating in the range 17 to 29 GHz has been demonstrated recently by Minnis [5]. The measured gain of the amplifier is approximately 3 dB. The cause of the low gain, which was not addressed, is predominantly due to gate and drain line attenuations caused by the device parasitic resistances. This amplifier was designed using the band-pass filter topology consisting of an inductor in the series arm and a parallel resonant circuit in the shunt arm. In this paper the classical constant-k topology consisting of series resonant circuit in the series arm and parallel resonant circuit in the shunt arm has been used. This topology has a superior transfer characteristic as compared to the one reported in [5].

We first present the analysis of the amplifier by modelling the gate and drain lines as constant-k ladder networks designed on the basis of image-parameter theory. The detrimental effects of the attenuations of the signals on the frequency response of the amplifier are considered and remedial measures are recommended. A millimeter-wave band-pass distributed amplifier is then designed and the results of computer simulations are presented.

II. ANALYSIS OF BAND-PASS DISTRIBUTED AMPLIFIERS

The schematic of a band-pass distributed amplifier is shown in Figure 1. The circuit topology differs from that of the conventional low-pass distributed amplifiers [1] in that it has inductors and capacitors in the series arms and inductors in shunt at the FET gates. We shall discuss in Section III the practical realization of the lumped components shown in Figure 1. An analytic model of the amplifier based on the modified (i.e., including the effects of the resistive elements in the amplifier model) constant-k theory will be presented in this section.

The principle of operation of the band-pass distributed amplifier does not differ from that of the conventional low-pass distributed amplifier [1]. The gate and drain lines in this case are designed to perform as band-pass filters. The lines are terminated by m-derived half-section filters (Figure 2) which provide the appropriate mid-series and mid-shunt image impedances at each section over a substantial portion of the pass-band.

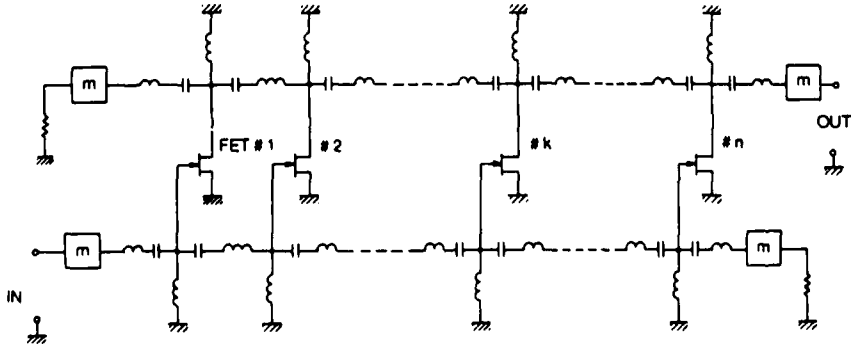
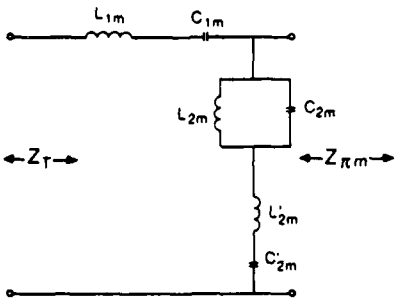


Figure 1 Schematic diagram of the band-pass distributed amplifier m: m-derived half-section filter



$$L_{1m} = \frac{m}{2} L_{1k}$$

$$C_{1m} = \frac{2C_{1k}}{m}$$

$$L_{2m} = \frac{2}{m} L_{2k}$$

$$C_{2m} = \frac{m}{2} C_{2k}$$

$$L'_{2m} = \frac{1 - m^2}{2m} L_{1k}$$

$$C'_{2m} = \frac{2m}{1 - m^2} C_{1k}$$

$$m \simeq 0.6$$

Figure 2 *m*-derived half-section filter

The gate and drain lines of the amplifier can be modelled using a simplified small signal unilateral circuit model of a GaAs FET [1] as shown in Figure 3(a) and (b). The gate- and drain-line sections are constant-k band-pass filters. The series and shunt arms of the sections resonate at the band center frequency ω_0 [6]. The phase shift a signal undergoes through gate- and drain-line sections can be shown to be

$$\phi_{g,d} \cong \cos^{-1}\left[1 - \frac{2(1 - x_k^2)^2}{x_k^2 \delta^2}\right] \text{rad} \qquad (1)$$

where $\phi_{g,d}$ is the phase shift through the gate- and drain-line sections, x_k $(= \omega/\omega_0)$ is the normalized frequency, and δ $(= (\omega_2 - \omega_1)/\omega_0)$ is the normalized bandwidth; ω_1 and ω_2 are the lower and the upper cutoff frequencies, respectively. In order that the currents flowing on the drain line toward the output terminals add in phase, one must design the amplifier such that $\phi_g = \phi_d$, which implies from Equation (1) that the value of δ must be made equal for gate and drain lines.

The equation for the magnitude of the voltage gain of the amplifier can be derived in a manner similar to that described in [1] and is given by

$$A \cong \frac{g_m \sqrt{R_{01} R_{02}} \sinh\left[\frac{n}{2}(A_g - A_d)\right] e^{-n(A_g + A_d)/2}}{2\left[1 - \frac{(1 - x_k^2)^2}{x_k^2 \delta^2}\right]^{1/2} \sinh\left[\frac{1}{2}(A_g - A_d)\right]} \qquad (2)$$

where g_m is the transconductance of the FETs, n is the number of FETs, R_{01} and R_{02} are the image impedances of the gate and drain lines at the band-center frequency, and A_g and A_d are the attenuations per section of the gate and drain lines, respectively.

Attenuation on the Gate Line. Consider the kth section of the gate line shown in Figure 3(a). The transfer characteristic of the section can be determined from the theory of image parameter networks [6]. When the attenuation (due to R_{gs}) is ≤ 0.4 Np it can be shown that

$$A_g \cong \frac{x_k^2 / \chi_g \delta}{\left[1 - \frac{(1 - x_k^2)^2}{x_k^2 \delta^2}\right]^{1/2}} \text{ Np} \qquad (3)$$

provided $|1 - x_k^2| \gg x_k^2/\chi_g^2 \ll 1$ and $\delta \geq |1/x_k - x_k|$. In the

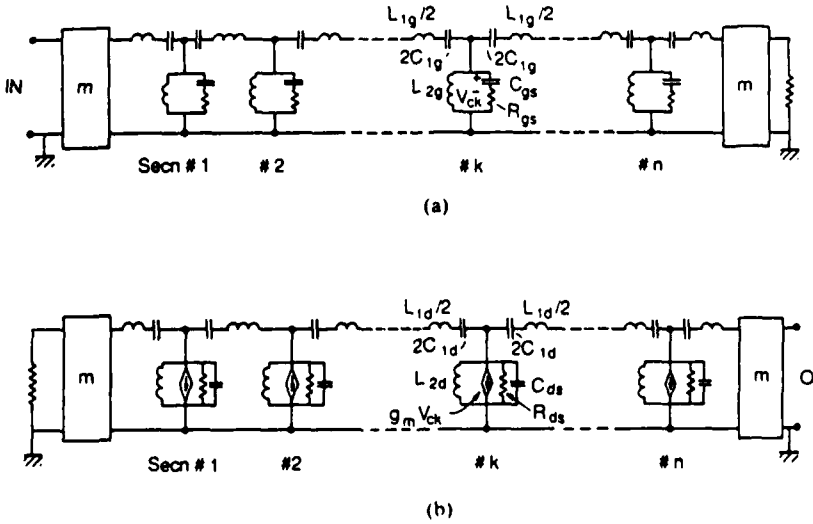


Figure 3 (a) Gate transmission line model. (b) Drain transmission line model

preceding equation, $\chi_g = \omega_g/\omega_0$ is the normalized gate RC circuit corner frequency; $\omega_g = 1/R_{gs}C_{gs}$.

The attenuation, A_g, as a function of normalized frequency is shown in Figure 4. The steep rise in attenuation predicted by (3) is clearly seen. The gate-line attenuation decreases the excitation of the transistors and thereby causes a severe roll-off of the gain vs. frequency response and limits the number of transistors in the amplifier. The increase in the mid-shunt image impedance near the cutoff frequencies causes the voltages at the transistor gates to increase, thereby compensating for the reduction in excitation. The rise in the image impedances of gate and drain lines near the cutoff frequencies can be seen in the following equation and Figure 5:

$$Z_{I\pi(g,d)} \cong \frac{R_0}{\left[1 - \dfrac{\left(1 - x_k^2\right)^2}{x_k^2\delta^2}\right]^{1/2}} \tag{4}$$

where R_0 is the image impedance at the band-center frequency.

At very high frequencies the loss-compensation provided by the rise in image impedances is insufficient in practical designs and other techniques will be addressed in Section III.

Attenuation on the Drain Line. The attenuation of the signal through a section of the drain line [kth section in Figure 3(b)] can be shown to be

$$A_d \cong \frac{\chi_d/\delta}{\left[-\dfrac{\left(1 - x_k^2\right)^2}{x_k^2\delta^2}\right]^{1/2}} \text{ Np} \tag{5}$$

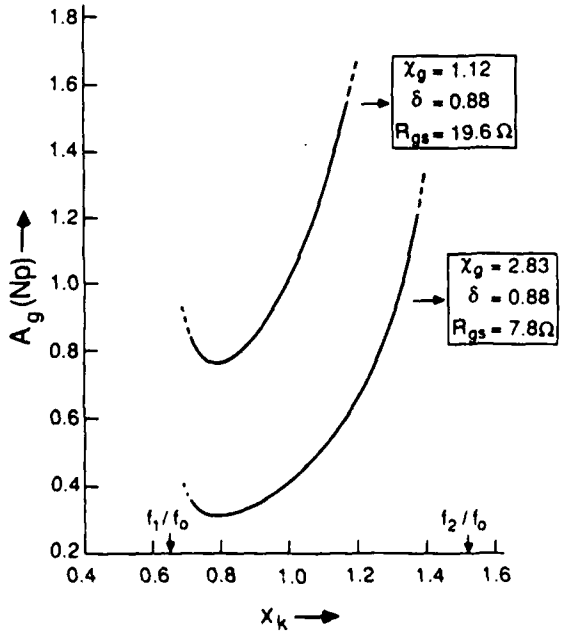


Figure 4 Attenuation per section of gate line vs. normalized frequency

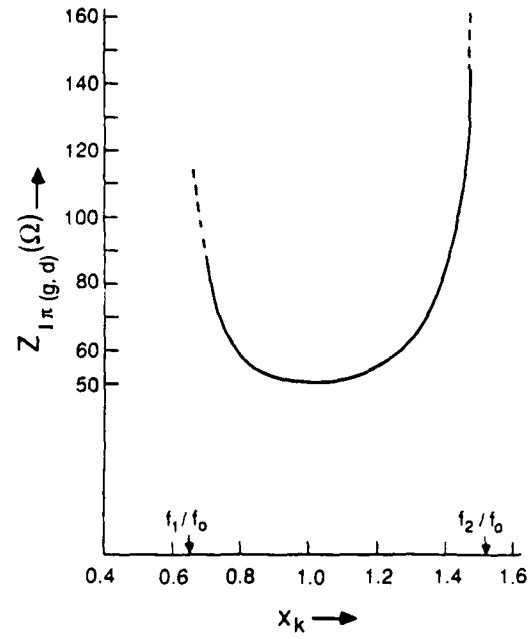


Figure 5 Gate- and drain-line π-section image impedance vs. normalized frequency

where χ_d ($= \omega_d/\omega_0$) is the normalized drain RC circuit corner frequency; $\omega_d = 1/R_{ds}C_{ds}$. The variation of drain-line attenuation with normalized frequency is shown in Figure 6. From the Figures 4 and 6 one can conclude that the drain-line attenuation is small and a slowly varying function of frequency over a substantial portion of the pass-band, in comparison to gate-line attenuation. Therefore the drain-line attenuation does not have as severe an effect on the amplifier frequency response and the number of allowable transistors as does the gate-line attenuation.

III. DESIGN OF BAND-PASS DISTRIBUTED AMPLIFIERS

The design and performance of band-pass distributed amplifiers will be illustrated in this section by means of an example. Consider the simplified equivalent circuit model of a InGaAs channel HEMT (0.1 × 100 μm) shown in Figure 7. The following design equations [6] can be used to compute the values of the circuit elements of the gate- and drain-line sections [Figures 3(a) and (b)] of the amplifier:

$$L_{1g}(\text{or } L_{1d}) = \frac{R_0}{\pi(f_2 - f_1)} \tag{6a}$$

$$C_{1g}(\text{or } C_{1d}) = \frac{f_2 - f_1}{4\pi R_0 f_1 f_2} \tag{6b}$$

$$L_{2g}(\text{or } L_{2d}) = \frac{R_0(f_2 - f_1)}{4\pi(f_2 f_1)} \tag{6c}$$

$$C_{2g}(\text{or } C_{2d}) = \frac{1}{\pi R_0(f_2 - f_1)} \tag{6d}$$

$$R_0 = \left[\frac{L_{1g}(\text{or } L_{1d})}{C_{2g}(\text{or } C_{2d})}\right]^{1/2} = \left[\frac{L_{2g}(\text{or } L_{2d})}{C_{1g}(\text{or } C_{1d})}\right]^{1/2} \tag{6e}$$

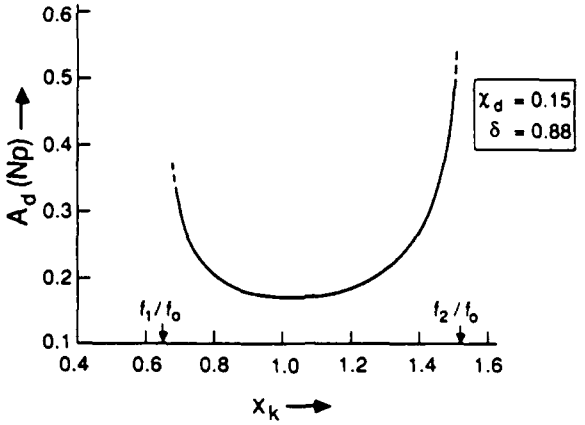


Figure 6 Attenuation per section of drain line vs. normalized frequency

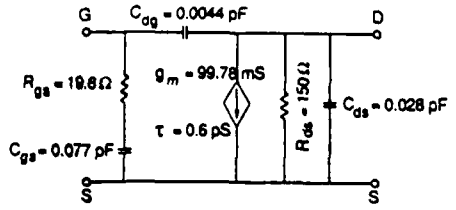


Figure 7 Simplified equivalent circuit model of 0.1 × 100-μm HEMT

where R_0 is the line image impedance at band center and f_1 and f_2 are the band-edge (cutoff) frequencies. The band-center frequency f_0 is given by

$$f_0 = (f_1 f_2)^{1/2} \tag{7}$$

For a specified f_0, the product $f_1 f_2$ is fixed [Equation (7)]. For a given R_0 and a given FET ($C_{2_g} = C_{g_s}$) the difference $f_2 - f_1$ is fixed [Equation 6(d)]. Therefore one can compute the frequencies f_1 and f_2. If the desired bandwidth is greater than $f_2 - f_1$ one must either decrease R_0 or decrease the effective C_{2_g} by connecting a capacitor in series with the gate [2]. It is interesting to note that $f_2 - f_1$ in Equation (6d) is replaced by the cutoff frequency f_c in the low-pass [1] case. Since f_0 can be greater than $f_2 - f_1$ it is clear that for a given FET (i.e., C_{g_s}) and R_0 it is possible to design band-pass amplifiers to operate beyond the low-pass cutoff frequency. This fact is illustrated in Figure 8 where the frequency responses of the amplifiers designed using the FET model in Figure 7 are shown. The low gain and the severe gain roll-off with frequency of the band-pass amplifier must be noted in Figure 8. This is predominantly due to gate-line attenuation. The gate-line attenuation caused by the gate-to-source parasitic resistances can be coun-

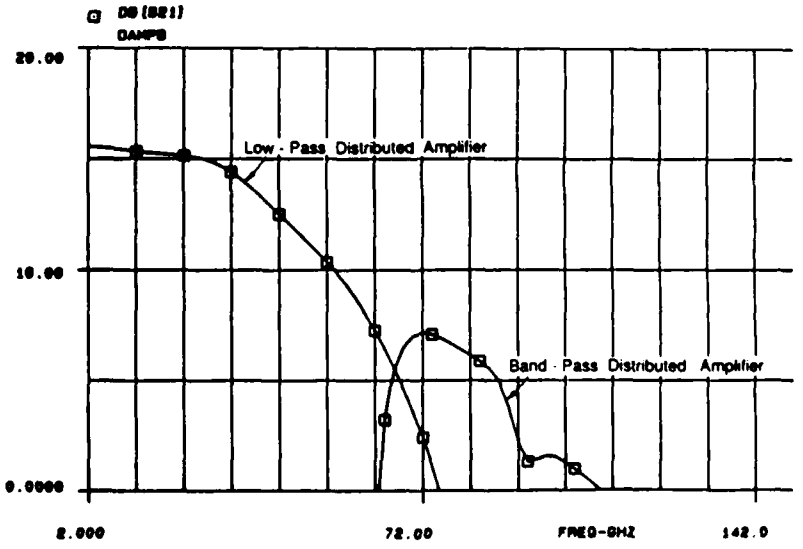


Figure 8 Gain vs. frequency responses of low-pass and band-pass distributed amplifiers

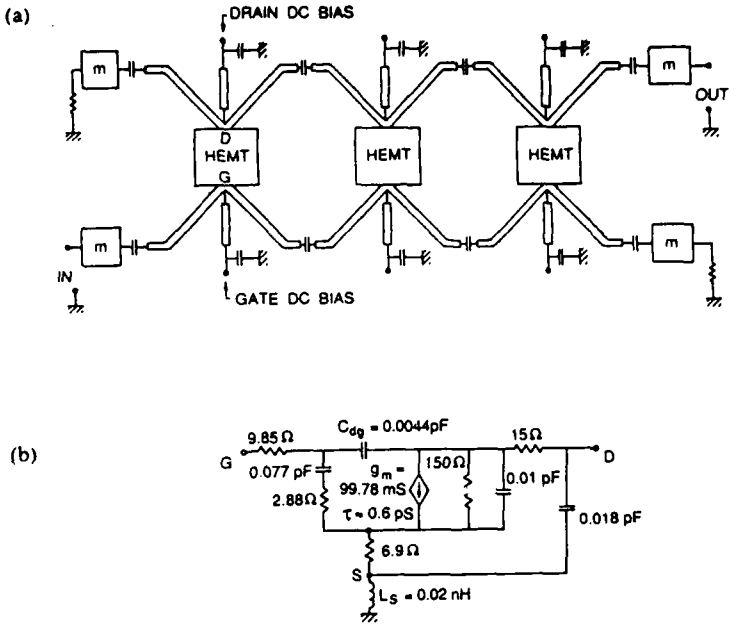


Figure 9 (a) Topology of the band-pass distributed amplifier. (b) Circuit model of the 0.1 × 100-μm HEMT

teracted by using negative resistance compensation [7]. Another technique to diminish gate-line attenuation is the use of series capacitors at the FET gates [2]. The reduction in attenuation enables one to increase the number of FETs in the amplifier which in turn increases the gain and output power. Further the attenuation compensation enables one to obtain flatter gain responses.

Design Example. In the design example here, f_0 = 94 GHz and R_0 = 50 Ω. Using the 0.1 × 100-μm device (circuit model in Figure 7) and the design equations (6a)–(6e) the following values for the circuit elements and band-edge frequencies are obtained: $L_{1g} = L_{1d}$ = 0.192 nH, $C_{1g} = C_{1d}$ = 0.014 pF, $L_{2g} = L_{2d}$ = 0.037 nH, f_1 = 61.34 GHz, and f_2 = 144.06 GHz.

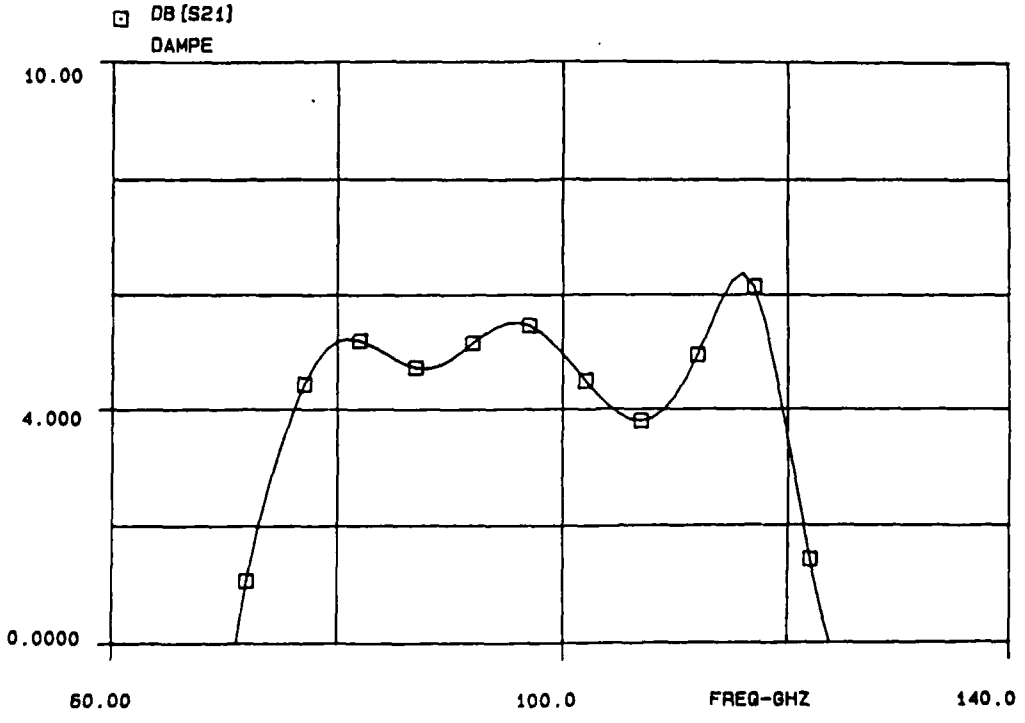


Figure 10 Gain vs. frequency response of the three-section band-pass distributed amplifier

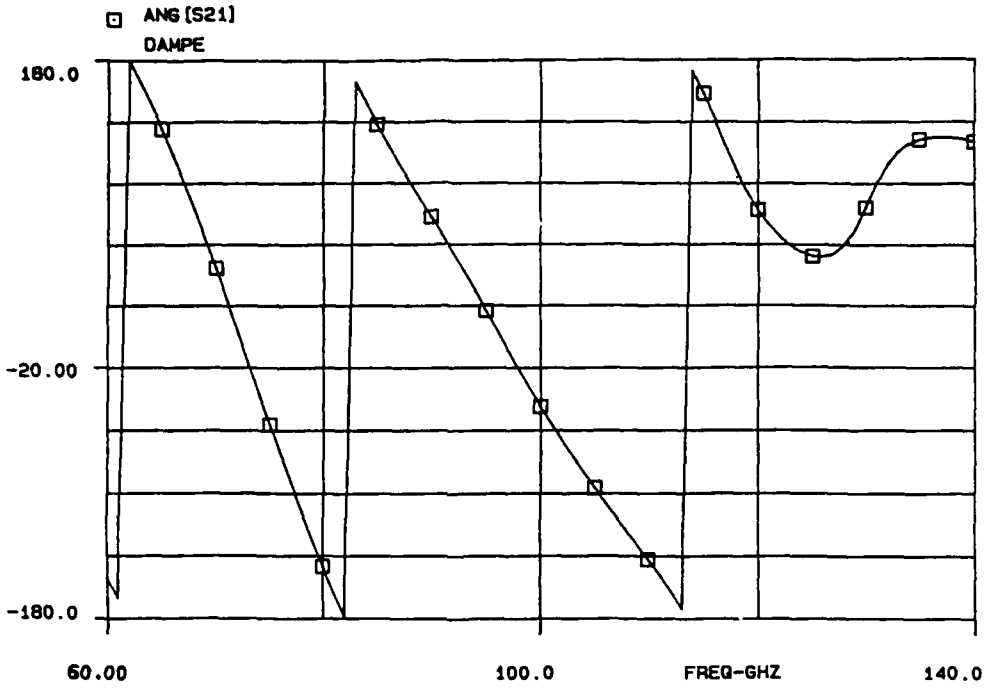


Figure 11 Phase vs. frequency response of the three-section band-pass distributed amplifier

The gate and drain lines were designed to have the same values of f_0 and $f_2 - f_1$. This ensures equal phase shifts for the gate- and drain-line sections [$\delta = f_2 - f_1/f_0$; the normalized bandwidth has to be equal for the lines according to (1)]. However, one can design the two lines to have different values for f_0 and $f_2 - f_1$ but the same value of δ. In this case the two lines together would behave like coupled stagger-tuned filters.

The topology of the band-pass distributed amplifier designed in this example is shown in Figure 9(a). The inductors in the design can be realized by means of short lengths of high impedance (90 Ω) microstriplines on 4-mil-thick SI GaAs substrate ($\epsilon_r = 12.9$). The capacitors in the series arms can be realized by means of interdigitated capacitors. The inductors in the shunt arms can be realized by means of short-circuit (terminated by capacitors) microstripline stubs. This allows one to bias the gate and drains of FETs as shown in Figure 9(a). The entire circuit is well suited for monolithic realization.

The amplifier topology shown in Figure 9(a) was optimized to obtain the required band-pass gain response centered around 94 GHz. The optimization was accomplished using Touchstone® circuit analysis software. The circuit element values were optimized keeping in mind the practical realizability of the components. During the optimization process it was found that the capacitance C_{d_g} of the FET, the via hole source grounding inductance L_s, and the parasitic resistances of the FET [Figure 9(b)] critically affected the gain response.

The gain and phase responses of the band-pass distributed amplifier are shown in Figures 10 and 11, respectively. The gain of the amplifier is 5 ± 1 dB in the frequency range from 76 to 119 GHz. The phase response in the frequency range is nearly linear. During optimization the negative resistance compensation effect was simulated by lowering the values of gate-to-source parasitic resistances. It was found that flatter gain responses are easier to accomplish over a narrower passband.

IV. CONCLUSIONS

The novel band-pass distributed amplifier design concept presented in this paper has demonstrated the feasibility of broadband GaAs monolithic distributed amplifiers for millimeter wave applications. The analysis of the amplifier indicates that the gate-line attenuation due to loading by the device parasitic resistances, severely affects the gain response.

ACKNOWLEDGMENT

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A RAPIDLY CONVERGENT GALERKIN-COLLOCATION (GC) METHOD FOR THE ANALYSIS OF ELECTROMAGNETIC SCATTERING FROM THIN-WIRE STRUCTURES

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KEY TERMS

Computational electromagnetics, thin-wire scattering, collocation, Galerkin, quadrature

ABSTRACT

Results obtained using a novel technique for computing the electromagnetic scattering from conducting thin-wire structures and which exhibit Galerkin-like convergence properties with collocation-like computational efficiency, are presented.

INTRODUCTION

The application of any numerical technique to the solution of the integral equation for scattering from conducting thin-wire structures discretizes it into the form of a matrix equation [1]. In electromagnetics the mnth term of the matrix representation of the operator (the impedance matrix) consists [2] of an integral, taken over the mth weighting segment, of the dot product of the mth weighting current ($\mathbf{J}_m$) and the electric field ($\mathbf{E}_n$) there due to the nth basis segment current ($\mathbf{J}_n$). Piecewise sinusoidal basis functions have always been an attractive option, since in this instance expressions for $\mathbf{E}_n$ are available in closed form [3]. A collocation method (Dirac delta weighting functions) used in conjunction with this choice of basis results in a numerical method that requires the minimum of computational effort to compute the impedance matrix elements (matrix fill computations). It has however been shown [4, 5] that the convergence rate of such a collocation method, and hence the method itself, is unsatisfactory. On the other hand, Butler and Wilton [5] have confirmed the rapid convergence of a Galerkin method which employs piecewise sinusoidal basis and weighting functions. This improvement is achieved at the cost of extended matrix fill computation (namely, numerical integration). It is apparent that an improved convergence rate requires increased computational effort in the determination of impedance matrix elements.

In this paper the results obtained from a novel approach, which will be referred to as the Galerkin-collocation (GC) method, are presented. This method requires a matrix fill computational effort on a par with that of the conventional collocation method, and yet demonstrates a convergence rate comparable to that of the Galerkin method.

THE GALERKIN-COLLOCATION (GC) METHOD

The GC method uses piecewise sinsusoidal basis functions, and thus the expressions for $\mathbf{E}_n$ are in closed form. The final integration required to evaluate the impedance matrix elements (as indicated in the previous section) is however performed using a customized Gaussian quadrature scheme. The latter scheme takes special care of the peculiar singularity of the free space Green's function that forms part of the integrand. This is done by deriving unique polynomials which are orthogonal (over each segment) with respect to the singular portion of this integrand. We have established that one or two quadrature points on each segment are sufficient to determine the matrix elements with sufficient accuracy. Use of three or more such points per segment offers negligible improvement over that with two. In what follows we will refer to the implementation of the technique with one and two points per segment as the GC-1 and GC-2 methods, respectively. As far as the number of computations per impedance matrix element is concerned, both GC-1 and GC-2 are essentially equivalent to that of the conventional collocation approach, with closed form expressions used to compute the impedance matrix elements. Nevertheless, as will be demonstrated below, the convergence properties of the GC method emulate those of the Galerkin method requiring a more elaborate and lengthy numerical integration scheme involving the numerical evaluation special functions [3].

NUMERICAL RESULTS

Results are presented here for three geometries that essentially form the *experimentum crucis* for thin-wire scattering. These

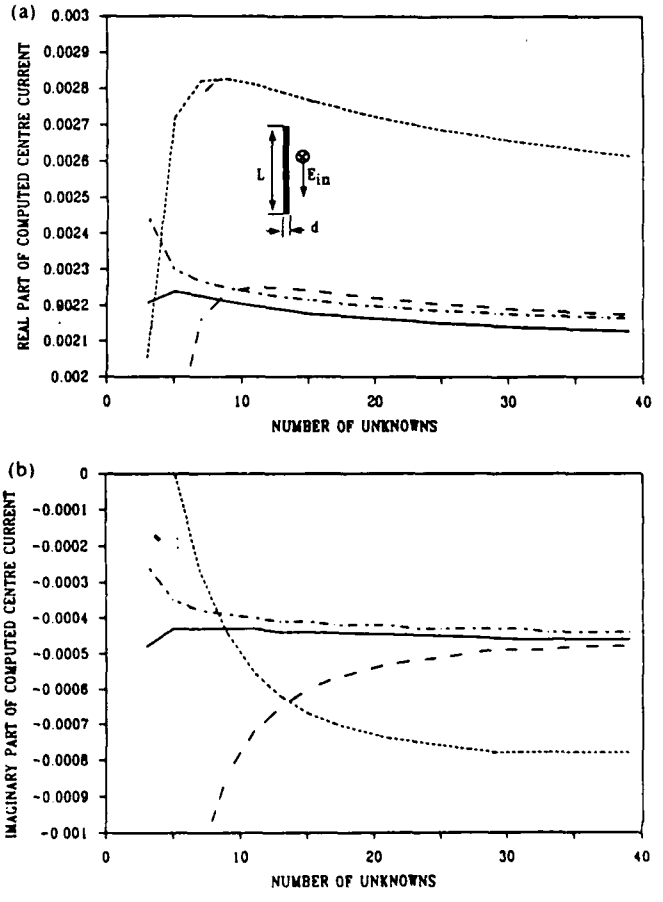

Figure 1 (a) Real part of the computed center current versus number of unknowns, for $L = 1.5\lambda$, $d = 0.002\lambda$, and incident polarization as shown. Galerkin method (——), conventional collocation method (·····), GC-1 method (– – –), and GC-2 method (–·–) (b) As for (a), but for imaginary part of the current